QTA1C04L2x000Exx

100G 10km QSFP28 LR4 Transceiver

Features

- ☑ Hot-pluggable QSFP+ form factor
- ☑ Power dissipation < 3.5W for up to 75 °C
- ☑ Support 100GBASE-LR4 and OTU4 4I1-9D1F
- ☑ Four LAN-WDM Chanels
- ☑ Support data transmission of 103.1 or 111.8Gb/s
- ☑ 10km reach over single mode fiber (SMF)
- ☑ 100G CAUI-4 electrical interface
- ☑ I^2C management interface
- ☑ RoHS 6/6 compliant
- ☑ Laser Class 1 IEC/CDRH compliant

Description

The QTA1C04L2x000Exx is a 100G hot pluggable fiber optic transceiver in the QSFP28 form factor. The transceiver is designed for 100GBASE-LR4 100G Ethernet application over up to 10km single mode fiber. Digital monitoring and control functions are supported via an I^2C serial interface per the Multi-Source Agreement (MSA) SFF-8636, Rev. 2.5.

The transceiver supports 100Gbps data rate over four local area network wavelength division multiplexed (LAN-WDM) lanes at 1295.56nm, 1300.05nm, 1304.58nm, and 1309.14nm. Each lane transmits and receives data streams at typical rate of 25.78125Gbps for 100GbE application or 27.952493Gbps for OTU4 4I1-9D1F applications. It provides an excellent solution for 100G data transmission over up to 10km single mode fiber. The low power consumption and excellent EMI performance enable system design with high port density. The product is designed and tested in accordance with industry safety standards. The transceiver is Class 1 Laser product per U.S. FDA/CDRH and IEC 60825 standards.

The QTA1C04L2x000Exx transceivers connect to standard 38-pin QSFP+ connectors for hot plug capability. This allows the system designer to make configuration changes or maintenance by simply plugging in different transceivers without removing the power supply from the host system. The transmitter and receiver DATA interfaces are internally AC-coupled.

The transceiver can be conveniently assembled into and released from the host system through a pull-tab.

The transceiver operates from a single +3.3V power supply over an operating case temperature range of 0°C to +75°C(Commercial) or -5°C to +85°C(Extended). The housing is made of metal for EMI immunity.

Absolute Maximum Ratings

Parameters		Symbol	Min	Max	Units
Supply Voltage Range		V_{CC}	- 0.5	+ 3.6	V
Case Operating Temperature	QTA1C04L2C000ExG	T_{OP}	0	+ 70	°C
	QTA1C04L2C000ExA		0	+ 70	
	QTA1C04L2E000ExG		- 5	+ 85	
Storage Temperature Range		T_{ST}	- 40	+ 85	°C
Operating Relative Humidity[1]		*RH*	0	85	%
Receiver Damage Threshold		P_{damage}	5.5	-	dBm
[1] Non condensing					

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Transmitter Performance Characteristics (Over Operating Case Temperature, VCC =3.13 to 3.47V)

Parameter		Symbol	Min	Typ	Max	Units
Signaling rate, each lane	100GbE	*B*	-	25.78125	-	Gb/s
	OTU4[1]		-	27.952493	-	
Lane wavelengths[2]		L_0	1294.53	1295.56	1296.59	nm
		L_1	1299.02	1300.05	1301.09	
		L_2	1303.54	1304.58	1305.63	
		L_3	1308.09	1309.14	1310.19	
Side mode suppression ratio		*SMSR*	30	-	-	dB
Total average launch power	100GbE	P_{avg_total}	-	-	+ 10.5	dBm
	OTU4		-	-	+ 10	
Average launch power, each lane[3]	100GbE	P_{avg}	- 4.3	-	+ 4.5	dBm
	OTU4		- 0.6	-	+ 4	
Optical Modulation Amplitude (OMA), each lane[4]		P_{OMA}	- 1.3	-	+ 4.5	dBm
Difference in launch power between any two lanes (OMA)		-	-	-	+ 5	dBm
Launch power in OMA minus TDP, each lane		-	- 2.3	-	-	dBm
Transmitter and dispersion penalty (TDP), each lane		*TDP*	-	-	+ 2.2	dB
Average launch power of OFF transmitter, each lane		P_{off}	-	-	- 30	dBm
Extinction ratio	100GbE	*ER*	4	-	-	dB
	OTU4		4	-	6.5	
$RIN_{20}OMA$		$RIN_{20}OMA$	-	-	- 130	dB/Hz
Optical return loss tolerance		-	-	-	20	dB
Transmitter reflectance		-			-12	dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		-	Compliant with IEEE 802.3ba {0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			

[1] OTU4 data rate is supported in QTAxC04L2x000E2G.
[2] The optical-electrical lanes mapping for the QTAxC04L2x000ExG is the following: L0↔Tx4; L1↔Tx3; L2↔Tx2; L3↔Tx1,
And The optical-electrical lanes mapping for the QTAxC04L2x000ExA is the following: L0↔Tx1; L1↔Tx2; L2↔Tx3; L3↔Tx4.
[3] Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[4] Even if the TDP < 1 dB, the OMA (min) must exceed this value.

Receiver Performance Characteristics (Over Operating Case Temperature, VCC =3.13 to 3.47V)

Parameter		Symbol	Min	Typ	Max	Units
Signaling rate, each lane	100GbE	*B*	-	25.78125	-	Gb/s
	OTU4[1]		-	27.952493	-	
Lane wavelengths[2]		L_0	1294.53	1295.56	1296.59	nm
		L_1	1299.02	1300.05	1301.09	
		L_2	1303.54	1304.58	1305.63	
		L_3	1308.09	1309.14	1310.19	
Average receive power, each lane[3]	100GbE	P_{input}	- 10.6	-	4.5	dBm
	OTU4		-6.9	-	+ 4	
Difference in receive power between any two lanes (OMA)		-	-	-	5.5	dBm
Receiver reflectance		-	-	-	- 26	dB
Receiver sensitivity (OMA), each lane	100GbE	P_{min}	-	-	- 8.6	dBm
Minimum equivalent sensitivity	OTU4		-		-8.4	dBm

Receiver 3 dB electrical upper cutoff frequency, each lane		-	-	31	GHz
Stressed receiver sensitivity (OMA), each lane @ 25.78125Gb/s (per Lane)[4]		-	-	- 6.8	dBm
LOS assert	*LOSA*	- 30	-	- 16.6	dBm
LOS de-assert	*LOSD*	-	-	- 13.6	dBm
LOS Hysteresis	-	0.5	-	-	dB

[1] OTU4 data rate is supported in QTA1C04L2x000E2G
[2] The optical-electrical lanes mapping is the following: L0↔Rx1; L1↔Rx2; L2↔Rx3; L3↔Rx4
[3] Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[4] Measured with conformance test signal as specified in IEEE 802.3ba

Transmitter Electrical Characteristics (Over Operating Case Temperature, VCC =3.13 to 3.47V)

Parameter	Symbol	Min	Typ	Max	Units
Differential Input Impedance	Z_d	-	100	-	Ω
Differential Input Voltage per lane	-	-	-	900	mV
Input impedance mismatch	-	-	-	10	%
Input High Voltage	V_{IH}	2.0	-	V_{cc}+0.3	V
Input LOW Voltage	V_{IL}	-0.3	-	0.8	V

Receiver Electrical Characteristics (Over Operating Case Temperature, VCC =3.13 to 3.47V)

Parameter	Symbol	Min	Typ	Max	Units
Differential voltage, pk-pk	*Vdiff*	-	-	900	mV
Common mode voltage	*Vcm*	- 350	-	2850	mV
Common Mode Noise, rms	-	-	-	17.5	mV
Differential Termination Resistance Mismatch (at 1 MHz)	-	-	-	10	%
Differential Return Loss (SDD22)	-	-	-	Per CEI-28G-VSR	dB
Common Mode to Differential conversion and Differential to Common Mode Conversion (SDC22, SCD22)	-	-	-	Per CEI-28G-VSR	dB
Common Mode Return Loss (SCC22) - from 250 MHz to 30 GHz	-	-	-	- 2	-
Transition Time: 20/80%	-	9.5	-	-	ps
Vertical Eye Closure	*VEC*	-	-	6.5	dB
Eye width at 10-15robability	*EW15*	0.57	-	-	UI
Eye height at 10-15 probability	*EH15*	228	-	-	mV

Power Supply Characteristics (Over Operating Case Temperature, VCC =3.13 to 3.47V)

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Voltage		V_{CC}	3.13	3.3	3.47	V
Power Consumption	QTA1C04L2C000ExG QTA1C04L2C000ExA	P_W	-	-	3.5	W
	QTA1C04L2E000ExG		-	-	4.0	

Laser Safety:

All transceivers are Class 1 Laser products per FDA/CDRH and IEC-60825-1:2007 & IEC60825-2:2004+A1+A2 standards. They must be operated under specified operating conditions.

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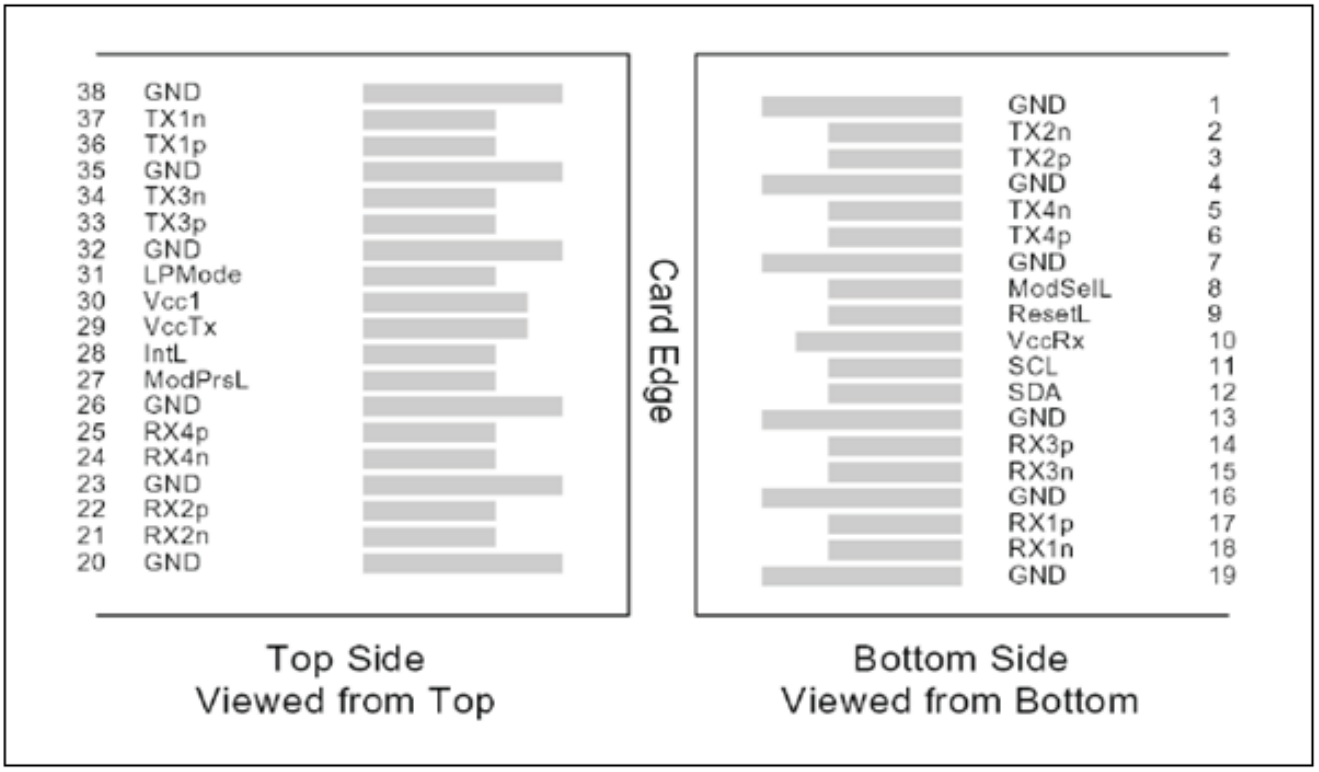
Oplink Communications, LLC.

This product complies with
21 CFR 1040.10 and 1040.11
Meets Class 1 Laser Safety Requirements

QSFP28 38-Pin Connector Pad Layout



Electrical Pin Definition

PIN	Logic	Symbol	Name / Description
1	GND	*GND*	Ground
2	CML	*Tx2n*	Transmitter Inverted Data Input
3	CML	*Tx2p*	Transmitter Non-Inverted Data Input
4	GND	*GND*	Ground
5	CML	*Tx4n*	Transmitter Inverted Data Input
6	CML	*Tx4p*	Transmitter Non-Inverted Data Input
7	GND	*GND*	Ground
8	LVTTL	*ModSelL*	Module Select
9	LVTTL	*ResetL*	Module Reset
10	VCC	*VCC_Rx*	+3.3V Receiver Power Supply
11	LVCMOS	*SCL*	2-wire Serial Interface Clock
12	LVCMOS	*SDA*	2-wire Serial Interface Data
13	GND	*GND*	Ground
14	CML	*Rx3p*	Receiver Non-Inverted Data Output
15	CML	*Rx3n*	Receiver Inverted Data Output
16	GND	*GND*	Ground
17	CML	*Rx1p*	Receiver Non-Inverted Data Output
18	CML	*Rx1n*	Receiver Inverted Data Output
19	GND	*GND*	Ground
20	GND	*GND*	Ground
21	CML	*Rx2n*	Receiver Inverted Data Output
22	CML	*Rx2p*	Receiver Non-Inverted Data Output
23	GND	*GND*	Ground
24	CML	*Rx4n*	Receiver Inverted Data Output
25	CML	*Rx4p*	Receiver Non-Inverted Data Output
26	GND	*GND*	Ground
27	LVTTL	*ModPrsL*	Module Present, grounded inside the module
28	LVTTL	*IntL*	Interrupt
29	VCC	*VCC_Tx*	+3.3V Transmitter Power Supply
30	VCC	*VCC1*	+3.3V Power Supply
31	LVTTL	*LPMode*	Low Power Mode, active high
32	GND	*GND*	Ground
33	CML	*Tx3p*	Transmitter Non-Inverted Data Input
34	CML	*Tx3n*	Transmitter Inverted Data Input
35	GND	*GND*	Ground
36	CML	*Tx1p*	Transmitter Non-Inverted Data Input
37	CML	*Tx1n*	Transmitter Inverted Data Input
38	GND	*GND*	Ground

Application Notes

Electrical interface: All signal interfaces are compliant with the QSFP28 MSA specifications. The high speed DATA interface is differential AC-coupled internally and can be directly connected to a 3.3V SERDES IC. Hardware control and status reporting pins include a 2-wire serial interface (SCL and SDA) and five 3.3V LVTTL hardware signals (ModSelL, ResetL, LPMode, ModPrsL, and IntL). The 2-wire interface pins are 3.3V LVCOMS compatible. Hosts shall use a 4.7 -10 kΩ pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL, SDA, and all low speed status outputs.

ModSelL: The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules

on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL: The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode: The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, and Power_set software control bits (Address A0h, byte 93 bits 0,1), the host controls how much power a module can dissipate. The allowed QSFP28 power consumption is shown in below truth table.

LPMode PIN State	Power_override bit	Power_set bit	Power Allowed
1	0	X	1.0W
0	0	X	3.5W
X	1	1	1.0W
X	1	0	3.5W

ModPrsL: ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL: IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

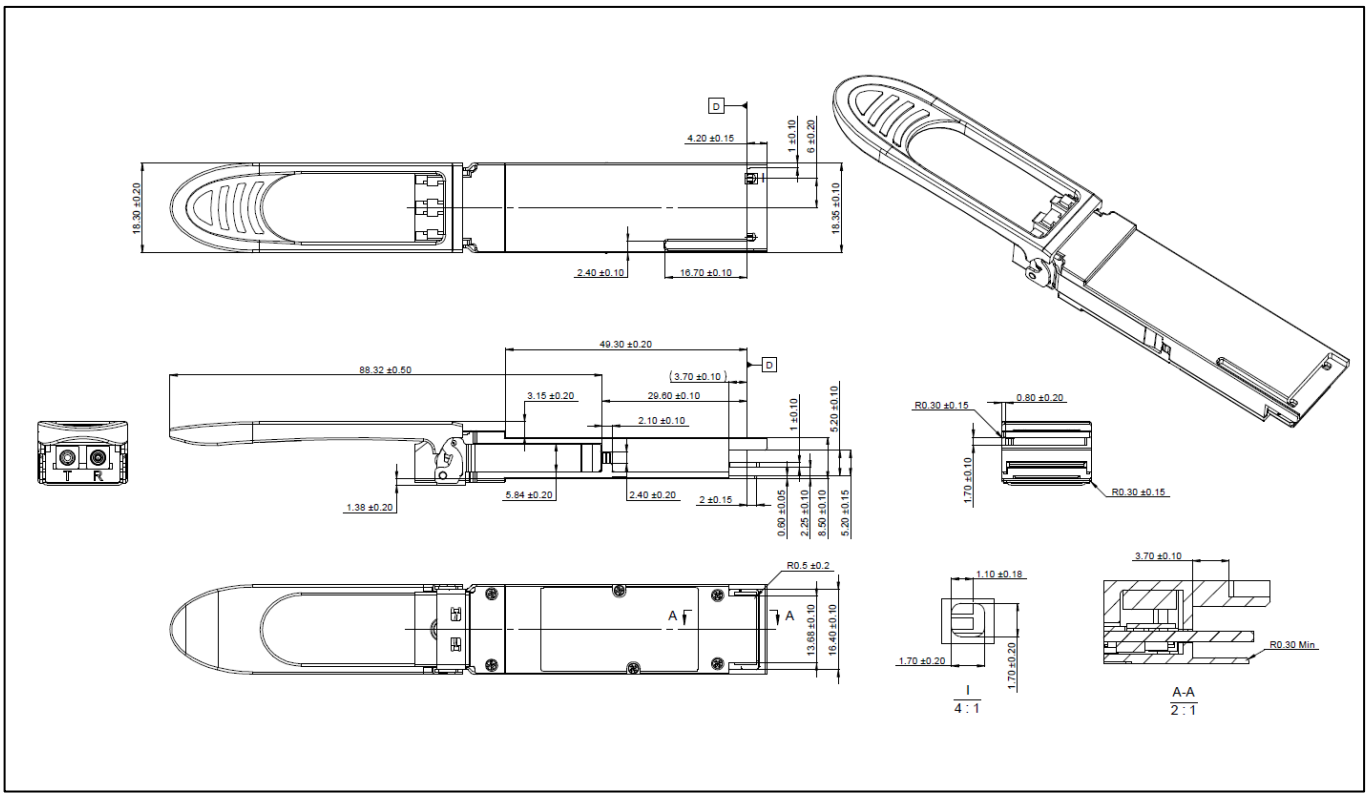
Two-wire Interface: The SCL (clock) and SDA (data) is a hot plug interface that may support a bus topology. SCL is the interface clock line and SDA is the bidirectional data line driven by both host and module depending upon the data directions. The data transfer protocol, signal characteristics, timing requirements, and the details of the mandatory and vendor specific data structures are defined in SFF-8679 and SFF-8636.

Upon module initialization, the alarm, control and monitor functions are available through the two-wire interface. Bytes in address 3 through 21 of A0h consist of interrupt flags for LOS, Tx Fault, warnings, and alarms. The non-asserted state shall be 0b. The per channel receiver LOS flags are A0h, address 3 bits 0~3 for channels 1~4 respectively. The transmitter fault flags are A0h, address 4 bits 0~3 for channels 1~4 respectively. Transmitter disable controls are through A0h address 86 bits 0-3 for channels 1-4 respectively, e.g. writing 1b disables the laser of the channel.

Power supply and grounding: The power supply line should be well-filtered. All power supply bypass capacitors should be as close to the transceiver module as possible.

The QSFP28 transceiver will power up in low power mode upon hot-plug, power cycle or reset. It will only reach fully functional operation after the host system enables “high power mode”.

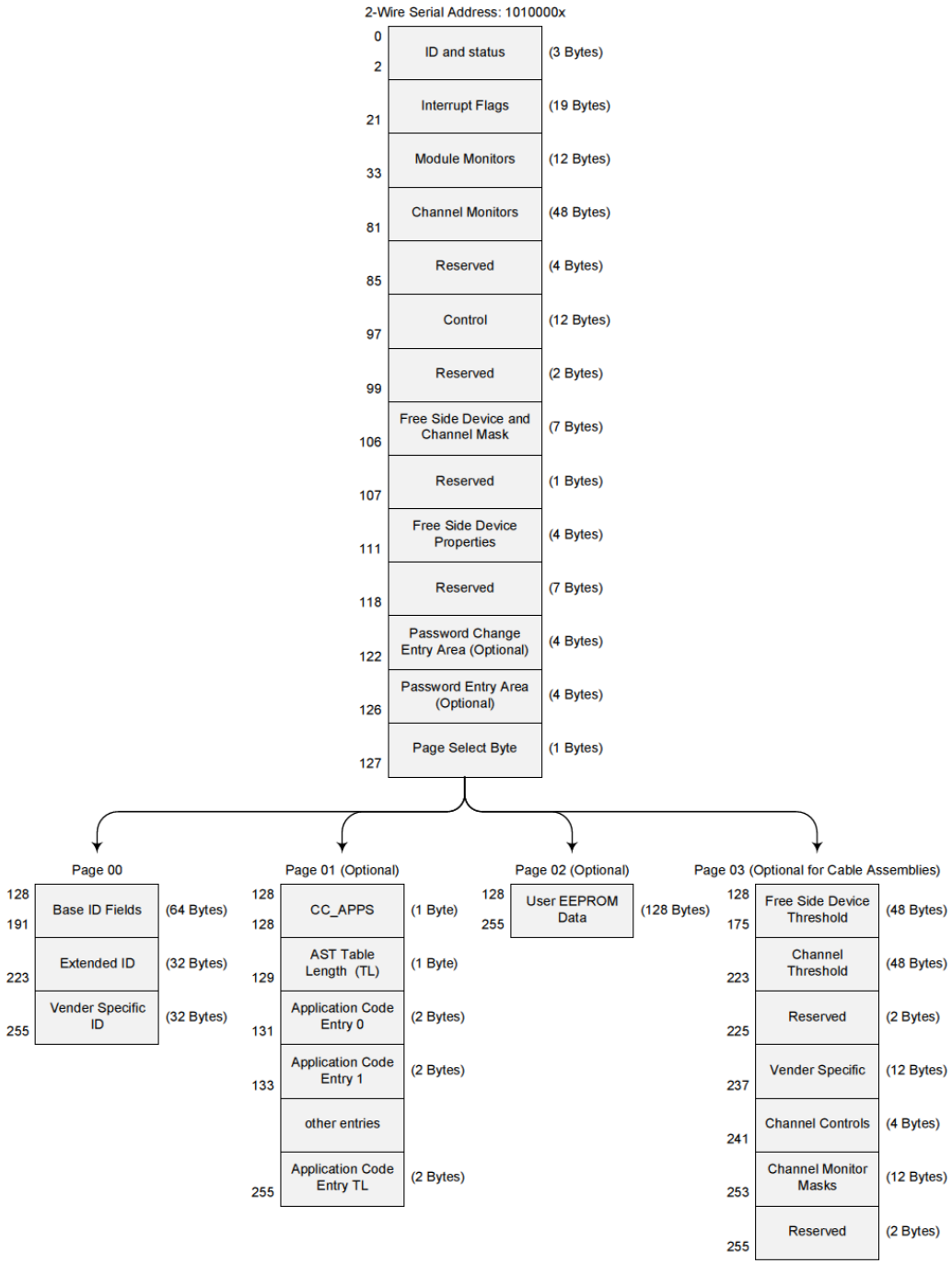
Module Outline



Interfacing the Transceiver

Host can determine the characteristic and status of the transceiver through a 2-wire common management interface. The interface also provides host a mechanism to control the operation of a module. SFF-8636 describes the interface details such as memory map and communication protocol used to transfer information between host and a module.

The common memory map is arranged into a single lower page address space (A0h) of 128 bytes and multiple upper address pages. The structure of the memory map is shown below. This structure permits timely access to addresses in the lower page such as interrupt flags and monitors. Less time critical entries such as serial ID information and threshold settings are available with the page select function.


2-Wire Serial Address: 1010000x
0
2
ID and status
(3 Bytes)
21
Interrupt Flags
(19 Bytes)
33
Module Monitors
(12 Bytes)
81
Channel Monitors
(48 Bytes)
85
Reserved
(4 Bytes)
97
Control
(12 Bytes)
99
Reserved
(2 Bytes)
106
Free Side Device and Channel Mask
(7 Bytes)
107
Reserved
(1 Bytes)
111
Free Side Device Properties
(4 Bytes)
118
Reserved
(7 Bytes)
122
Password Change Entry Area (Optional)
(4 Bytes)
126
Password Entry Area (Optional)
(4 Bytes)
127
Page Select Byte
(1 Bytes)
Page 00
128
191
Base ID Fields
(64 Bytes)
223
Extended ID
(32 Bytes)
255
Vender Specific ID
(32 Bytes)
Page 01 (Optional)
128
128
CC_APPS
(1 Byte)
129
AST Table Length (TL)
(1 Byte)
131
Application Code Entry 0
(2 Bytes)
133
Application Code Entry 1
(2 Bytes)
other entries
255
Application Code Entry TL
(2 Bytes)
Page 02 (Optional)
128
255
User EEPROM Data
(128 Bytes)
Page 03 (Optional for Cable Assemblies)
128
175
Free Side Device Threshold
(48 Bytes)
223
Channel Threshold
(48 Bytes)
225
Reserved
(2 Bytes)
237
Vender Specific
(12 Bytes)
241
Channel Controls
(4 Bytes)
253
Channel Monitor Masks
(12 Bytes)
255
Reserved
(2 Bytes)

Ordering Information

Oplink PN	Operating Temperature	Nominal Wavelength(nm)	Data Rate (Gb/s)	Distance	Latch System
QTA1C04L2C000E1G	0˚C to + 70˚C	1295.56, 1300.05, 1304.58, 1309.14	103.125	10km	Pull-tab
QTA1C04L2C000E1A	0˚C to + 70˚C	1295.56, 1300.05, 1304.58, 1309.14	103.125	10km	Pull-tab
QTA1C04L2E000E1G	-5˚C to + 85˚C	1295.56, 1300.05, 1304.58, 1309.14	103.125	10km	Pull-tab
QTA1C04L2C000E2G	0˚C to + 70˚C	1295.56, 1300.05, 1304.58, 1309.14	103.125 and 111.809	10km	Pull-tab
QTA1C04L2E000E2G	-5˚C to + 85˚C	1295.56, 1300.05, 1304.58, 1309.14	103.125 and 111.809	10km	Pull-tab