Reducing Development Risk in Communications Applications with High-Performance Oscillators

Introducing Silicon Labs' new Ultra Series™ Oscillators

Powered by 4th Generation DSPLL Technology, new oscillator products address 25/40/50/100/400Gbps timing challenges

As communications and data center applications transition to higher data rates to support rapidly increasing Internet traffic demands, SerDes reference clock performance is becoming increasingly important. If reference clock jitter is too high, it results in unacceptably high system bit-error rate (BER), lost traffic or loss of system communication. In addition, 56G PAM4 PHYs, 100G/200G/400G Ethernet, and 100G/400G OTN require a diverse mix of frequencies, further increasing timing complexity.

High-Speed Communications and Data Center Timing Requirements

Silicon Labs' latest Si54x Ultra Series oscillator products are purpose-built for these demanding high-speed communications and data center applications. These high performance oscillators offer any-frequency synthesis, ultra-low jitter of 80 fs RMS and are available in standard, small form factor oscillator footprints. By providing best-in-class jitter margin and frequency flexibility, our Ultra Series makes it easy for hardware designers to design with confidence and de-risk product development.

Figure 1. High-Speed Communications and Data Center Timing Requirements

Standard	Data Rate	Target Frequencies	Reference Clock Max Phase Jitter*
CEI-28G	28Gbps	106.25MHz 125.00MHz 156.25 MHz 161.13281 MHz 175 MHz 200 MHz 322.265625 MHz 644.53125 MHz	150fs
CEI-56G PAM4	56Gbps		150fs
100G Ethernet	4x25.8Gbps		180fs
CAUI-4	4x25.8Gbps		240fs
16G Fibre Channel	14.0Gbps		240fs
32G Fibre Channel	25.6Gbps		130fs
Infiniband EDR	25.8Gbps		180fs
Rapid IO – 4	25.3125Gbps		290fs
SONET OC-192	9.953Gbps		240fs

*Note: Calculated directly from reference clock or transmitter eye closure specifications budgeting eye closure 50/50 deterministic/rms and 33%/67% clock/transmitter per raw (pre-FEC) BER requirements.

Ultra Series DSPLL Architecture

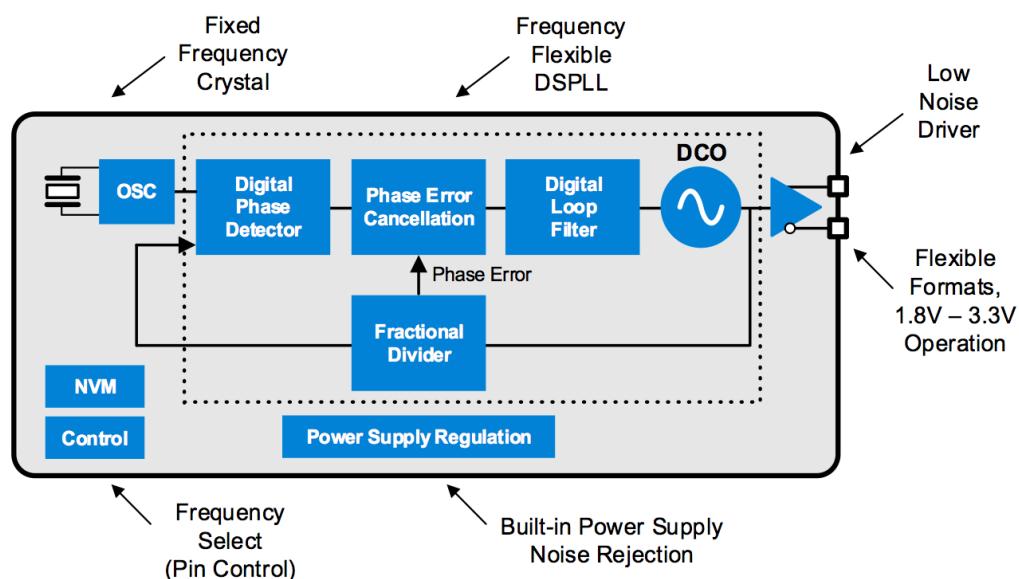Figure 2. Ultra Series DSPLL Architecture

Figure 2 provides a high-level overview of Silicon Labs' new Ultra Series 4th generation DSPLL architecture. Unlike traditional oscillator approaches that require complex batch manufacturing processes and different crystals for different frequencies, the Si54x architecture combines a simple, high quality fixed frequency crystal and Silicon Labs' latest generation DSPLL to produce any frequency. The device is programmed and customized to the target frequency during outgoing test. Using this innovative approach the Si54x can be easily mass customized to meet each customer's unique requirements. The Si54x Ultra Series supports any frequency from 200 kHz to 1.5 GHz, enabling a single product family to support both standard and custom frequency applications with ease.

Designed in industry-leading 55 nm CMOS technology, the 4th generation DSPLL leverages a highly digital architecture to deliver best-in-class frequency flexibility and jitter performance. The input to the DSPLL's phase detector is converted from analog to digital, enabling the DSPLL to operate entirely in the digital domain. This all-digital approach has multiple benefits. First, the Digitally-Controlled Oscillator (DCO) can be precisely steered with a step size as small as < 1 ppb to track out phase delay between the reference and feedback clocks. The DCO gain is small, making the circuit less susceptible to noise than conventional analog PLLs. Secondly, the DSPLL supports an innovative phase error cancellation circuit that uses advanced digital signal processing to remove PLL noise due to delay, non-linearity, and temperature effects. These architectural features ensure consistent device performance across process, voltage and temperature. As a result, Silicon Labs' 4th generation DSPLL architecture delivers ultra low jitter across the entire operating range.

Frequency Flexibility with Ultra-Low Jitter

The graph below shows the Ultra Series jitter performance versus operating frequency and temperature. Two performance grades are available. The Si545/6/7 devices provide phase jitter performance of 80 fs RMS typical (12kHz – 20MHz), whereas the Si540/1/2 devices provide jitter performance of 125 fs RMS typical (12kHz – 20MHz). Given their jitter performance, the Si54x maximizes jitter margin and enables customers to design with confidence.

**Figure 3. Si54x Ultra Series XO Jitter Performance vs Frequency**
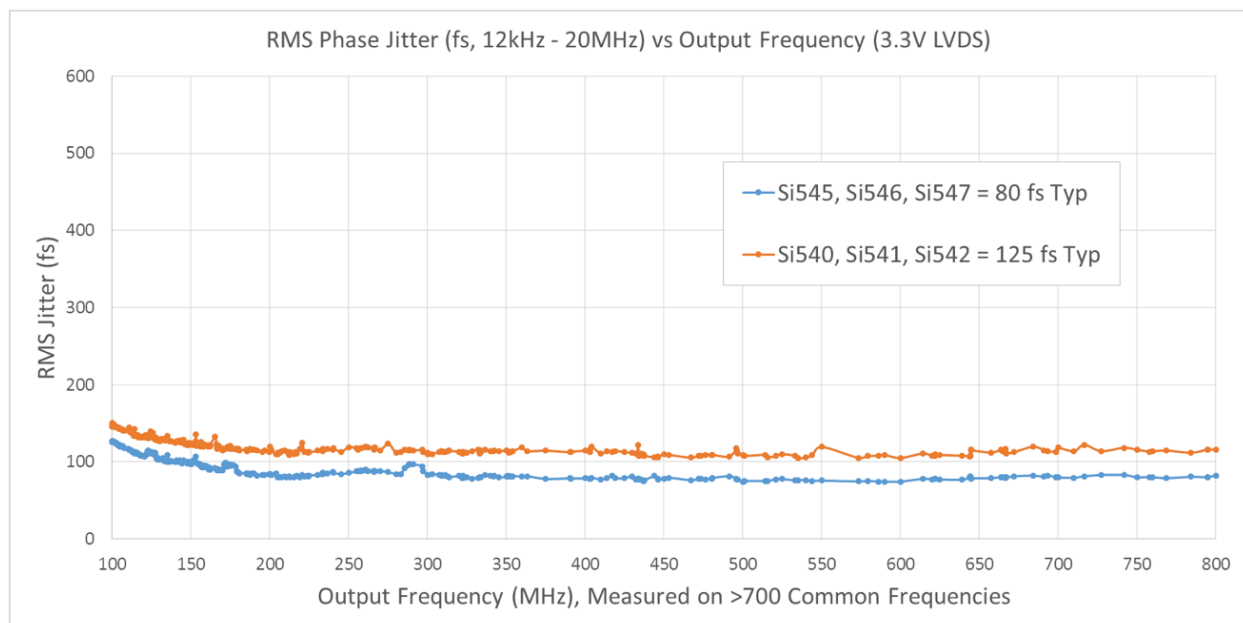
To further simplify device evaluation, Silicon Labs offers an XO Phase Noise Lookup Utility that can be used to retrieve >1000 measured phase noise plots of Silicon Labs oscillators across a wide range of popular frequencies. See http://www.silabs.com/tools/pages/oscillator-phase-noise-lookup-tool.aspx to use this free utility.

Integrated Power Supply Noise Regulation

The 4th generation DSPLL has an extensive network of on-chip low drop out regulators to provide power supply noise rejection, ensuring consistently low jitter operation even in noisy system environments. Another benefit of integrated power supply noise regulation is simplified power supply filtering, PCB design and layout.

Figure 4. Integrated PSNR Minimizes Additive Jitter
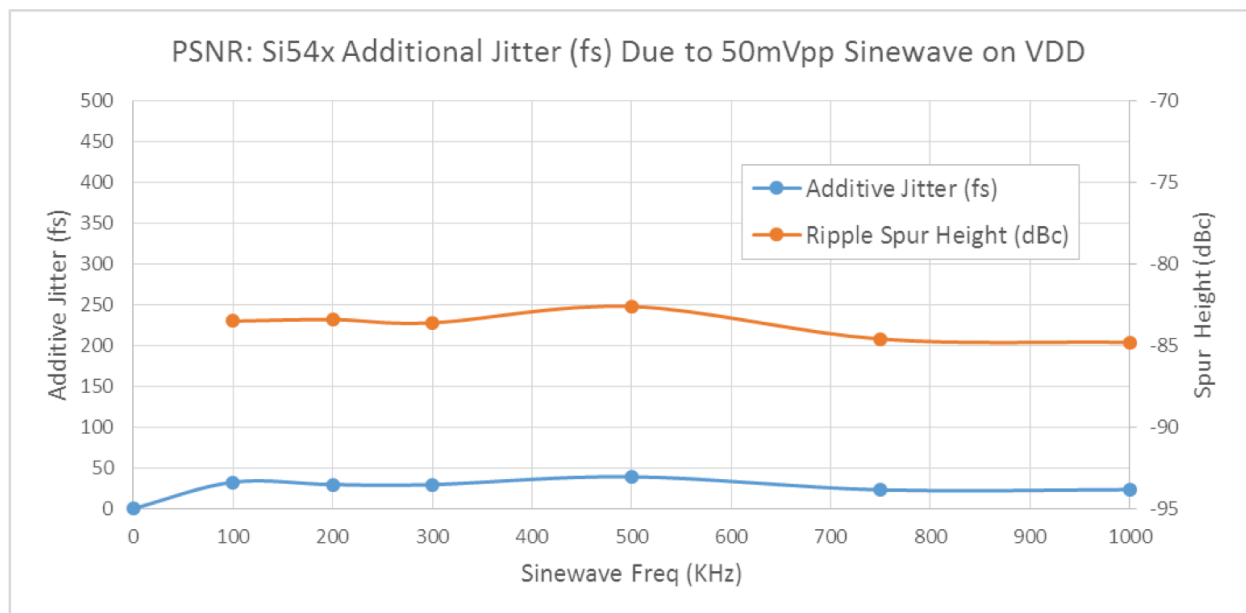
Multi-Frequency Support

In addition to standard single frequency oscillators, dual and quad frequency oscillators leveraging Silicon Labs' 4th generation DSPLL architecture are available. These devices can replace two or more discrete oscillators with a single IC, minimizing BOM cost and complexity. There are multiple benefits of multi-frequency oscillators:

- Support multi-protocol SerDes with single device
- Simplified set up / hold time testing
- Frequency margining (e.g. 156.25 MHz + 50 ppm, 156.25 MHz, 156.25 MHz -50 ppm)
- Simplified prototyping. Test new SerDes and ASICs with a variety of reference clocks using a multi-frequency oscillator. Transition to a fixed, single frequency oscillator once the final frequency is selected.

Wide Range of Format Options with Single Voltage Supply

Silicon Labs' Ultra Series oscillators have a highly flexible output driver that can be factory customized to support any common signaling format: LVDS, LVPECL, HCSL, CML, CMOS and dual CMOS. In addition, the output driver supports a wide supply voltage range. A single Si54x device can support 1.8V-3.3V operation, enabling a single part number to replace multiple fixed-voltage 1.8V, 2.5V and 3.3V oscillators.

Quick-Turn Samples

Silicon Labs offers a web-based utility to create custom oscillators in < 1 minute. Once a part number is created, an order can be placed with a Silicon Labs franchised distributor or via Silicon Labs' website. Samples typically ship 1-2 weeks after order placement. This process greatly simplifies oscillator procurement and is an excellent way to get quick-turn devices for prototypes and NPI builds. Silicon Labs' web-based part number utility is available at http://www.silabs.com/tools/pages/utilityintro.aspx

Visit http://www.silabs.com/oscillators for more information about Silicon Labs oscillator products.