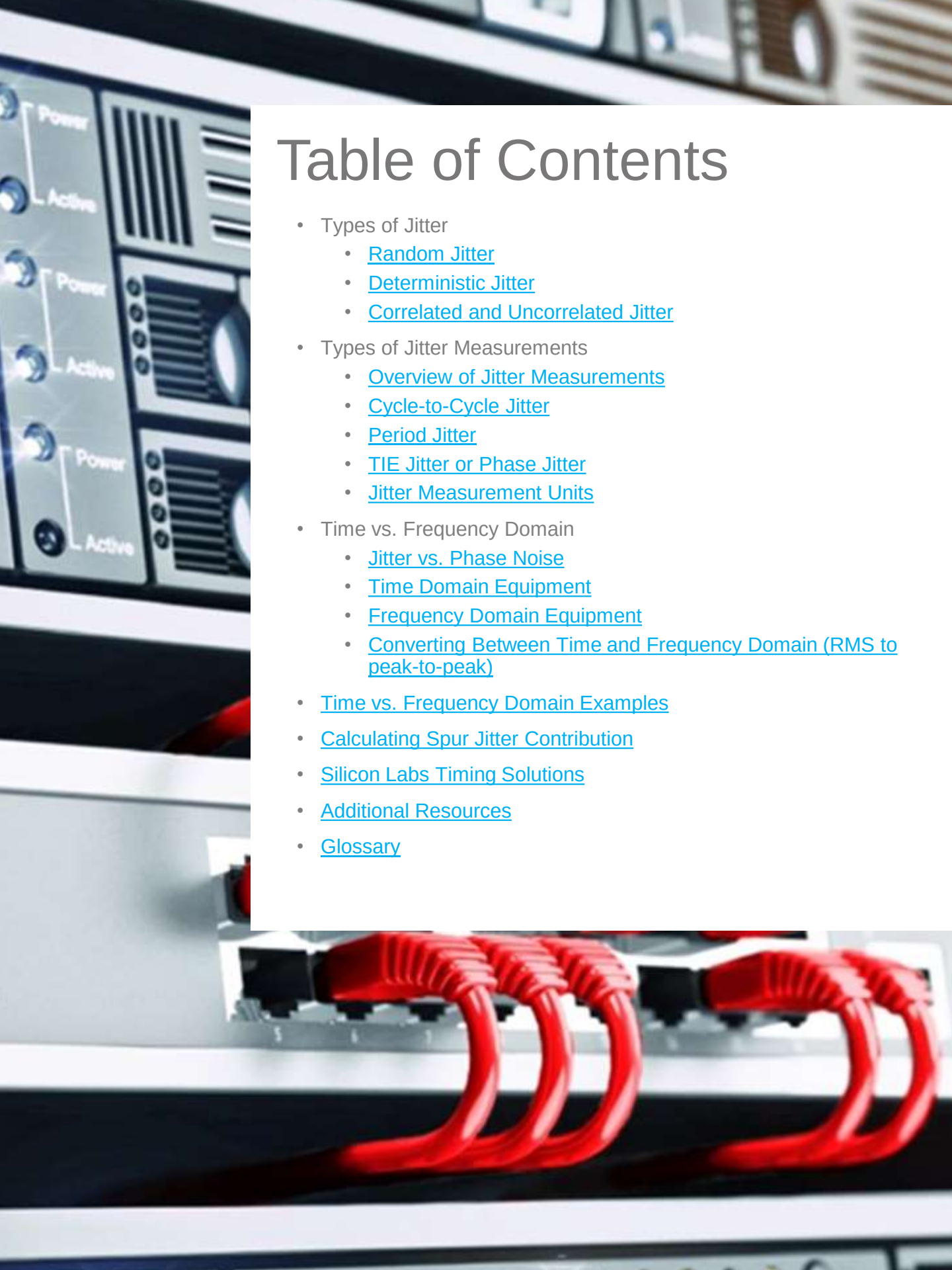
Timing Jitter Dictionary & Measurement

Silicon Labs Timing



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Introduction

The demand for near instant data access is increasing exponentially. High data rate applications like video, in conjunction with growing numbers of devices connected to each other, the Cloud and the Internet, are driving usage ever higher. Likewise, users expect to upload and download high-density data in real-time, abandoning web sites almost immediately if the speed is slow.

These trends are increasing the need for higher speed, higher bandwidth networks with higher data rates, and faster data interfaces. As speeds increase, the clocks and timing components that support them must provide better timing sources.

Jitter is the measure of timing performance. High jitter means poor timing performance in most cases.

This primer provides an overview of jitter and offers practical assistance in taking jitter measurements.

Types of Jitter

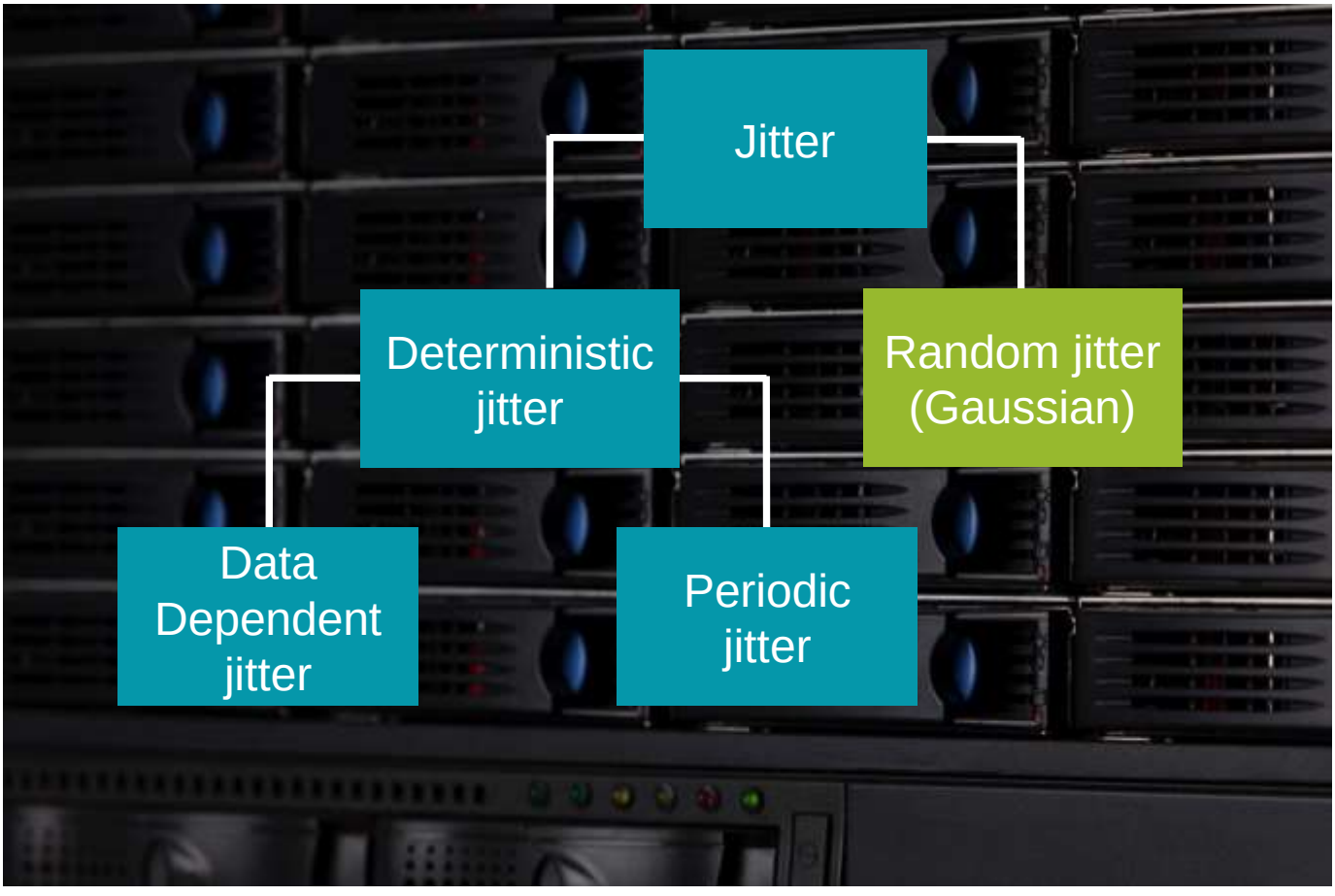
Jitter falls into two broad categories: random jitter and deterministic jitter*.

Random Jitter

Random jitter is a broadband stochastic** Gaussian process that is sometimes referred to as “intrinsic noise” because it is present in every system. In the various phase noise plots shown later in this document the relatively smooth sections along the bottom represent the intrinsic noise floor and are indicative of random jitter.

*Links to additional, more detailed information is available in the documents referenced in the Additional Resources page.

**Words in blue are defined in the glossary.



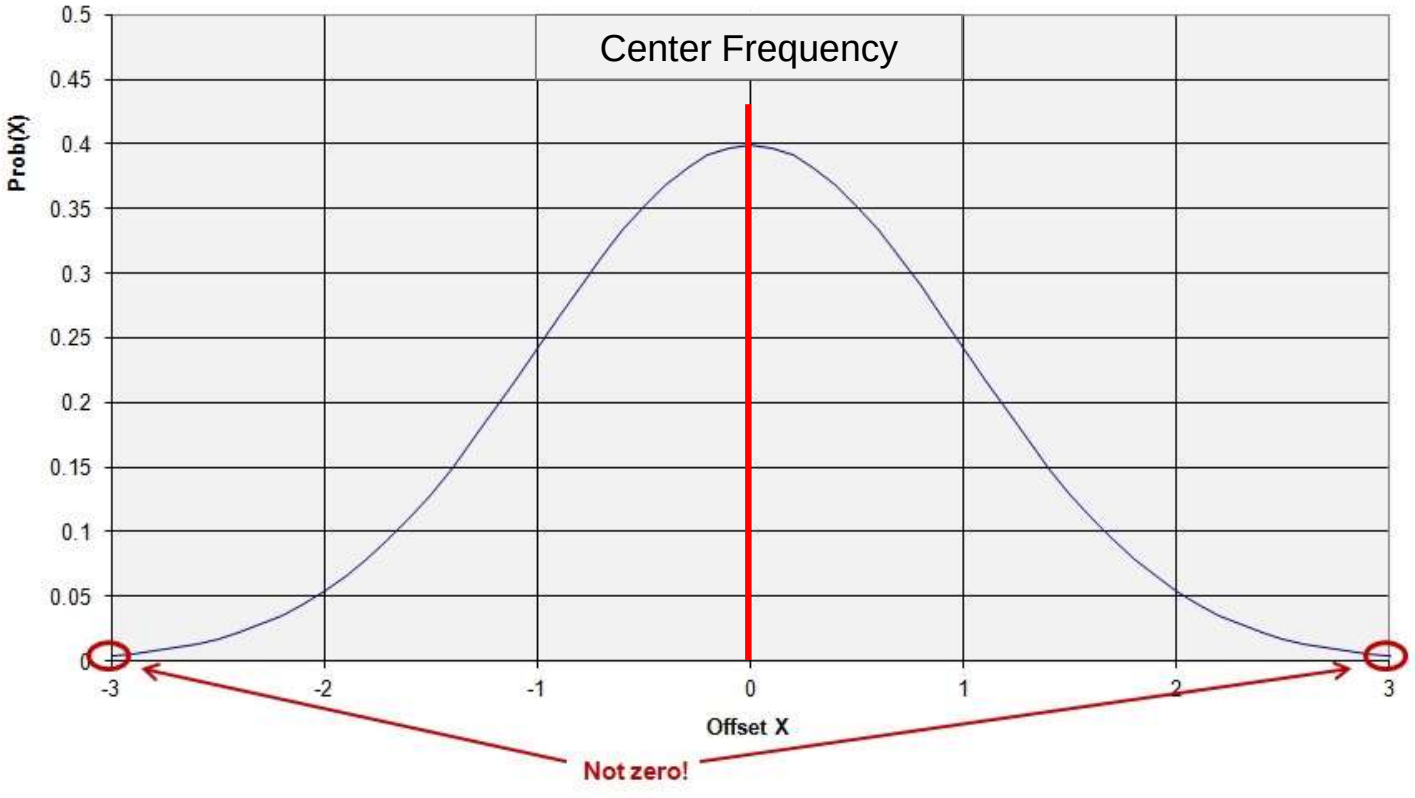
Types of Jitter

Random jitter's instantaneous noise value is mathematically unbounded. Looking at the random jitter Gaussian curve below, the two tails extending away from the center approach zero, but never fully reach it.

Although the probability of some values is very small, it is not zero, and therefore unbounded.

Random jitter can be a significant contributor to overall system jitter. However, it is unbounded and intrinsic to each system and is hard to diagnose and remedy.

Gaussian Distribution of Random Jitter



Types of Jitter

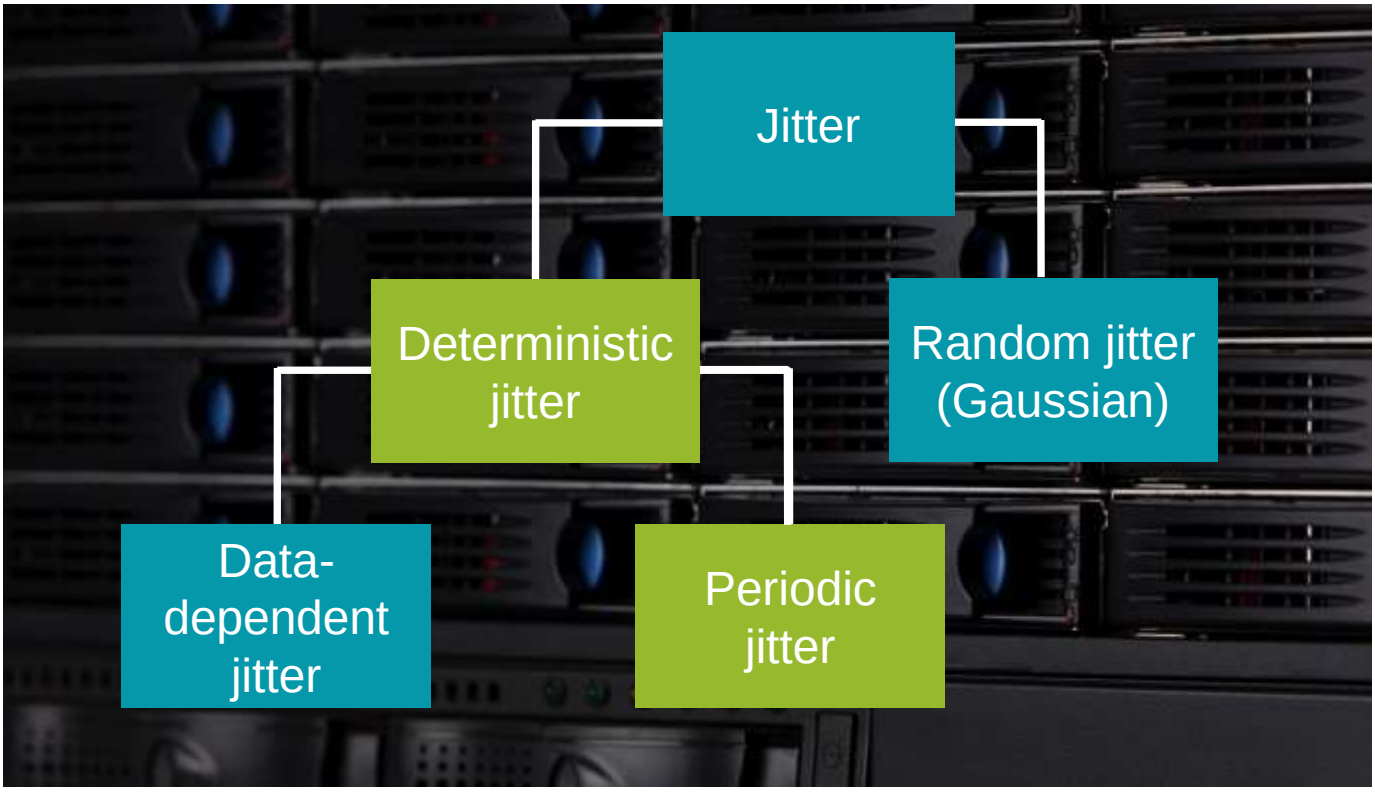
Deterministic Jitter

Deterministic jitter is not random or intrinsic to every system. It has a specific cause and is often periodic and narrowband. This means it is repetitious at one or more frequencies. Therefore, deterministic jitter is typically identifiable and can be remedied.

Deterministic jitter can be further subclassified into periodic jitter and data-dependent jitter. Jitter from a switching power supply is periodic and deterministic because it has the same, periodic frequency as the switching power supply.

In contrast, intersymbol interference (ISI) is an example of data-dependent jitter from an isochronous 8B/10B coded serial data stream (e.g., Ethernet or PCI Express). These protocols use dynamically changing duty cycles and irregular clock edges, which contribute to overall jitter.

Data-dependent jitter measurement varies by system, functionality, and other factors, and are not specifically addressed in this document.



Types of Jitter

Correlated and Uncorrelated Jitter

Correlated jitter on a clock is deterministic and always caused by and correlated to a noise source. An example of correlated jitter is periodic jitter, as in the case of a system power supply. However, correlated jitter can be aperiodic. An example of correlated aperiodic jitter is interference on a clock from a serial line. The interference is correlated to the serial data line, but the serial data may be either periodic or aperiodic.

Uncorrelated jitter is not statistically connected to an identifiable noise source. Random jitter is always uncorrelated; however, some correlated jitter may appear to be uncorrelated or random. This may occur when several noise sources overlap one another, causing their correlated jitter to appear uncorrelated. These noise sources are often difficult to identify.

Uncorrelated Jitter

- Intrinsic noise present in every system
- Also known as random jitter
- Statistically unrelated to an identifiable noise source
- Can be a significant contributor to overall system jitter

Correlated Jitter

- Statistically identifiable as coming from a specific noise source
- Typically periodic but can also be aperiodic, making it difficult to diagnose
- More than one noise source may cause correlated jitter seem uncorrelated

Types of Jitter Measurements

Overview – Types of Jitter Measurements

At a high level, there are three primary measurements for clock jitter. Each type of measurement applies to various applications with different timing performance requirements.

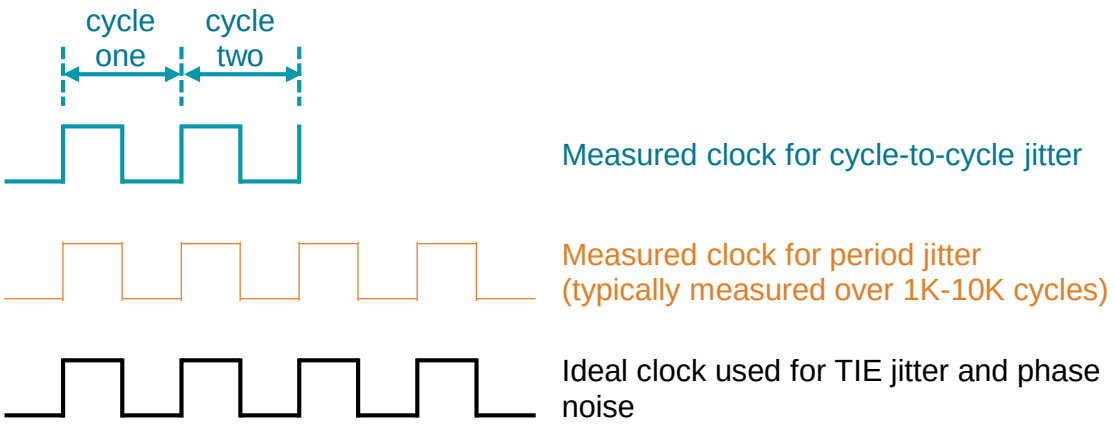
Applications with the most stringent requirements almost always specify maximum Time Interval Error (TIE) jitter and phase noise, and may include requirements for period jitter and cycle-to-cycle jitter as well.

TIE jitter and phase noise measurements require an ideal clock to compare against. These two measurements indicate the minimum, typical and maximum difference between an ideal clock and the measured clock.

Period jitter and cycle-to-cycle jitter are useful for digital designers concerned with timing for set-up and hold times within digital systems.

Period jitter measures the clock across a large number of its own cycles and provides the minimum, typical and maximum difference compared to the statistical mean of those measurements.

Cycle-to-cycle jitter measures the delta from one clock period to its adjacent clock period. Again, this is useful for digital designers who are concerned with set-up and hold times in digital design.



Types of Jitter Measurements

Cycle-to-Cycle Jitter

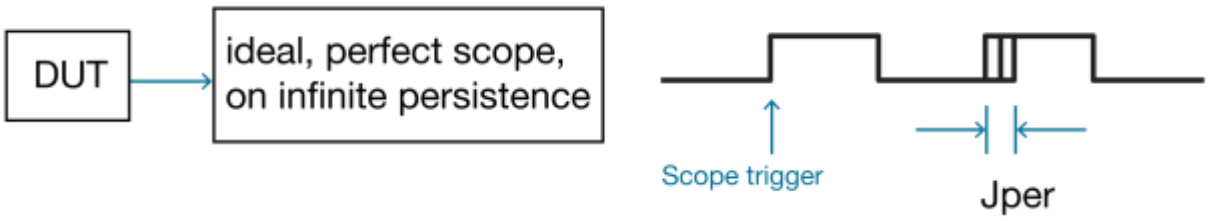
Peak cycle-to-cycle jitter is the maximum difference between consecutive, adjacent clock periods measured over a fixed number of cycles, typically 1,000 cycles or 10,000 cycles. Cycle-to-cycle jitter is used whenever there is a need to limit the size of a sudden jump in frequency.

The term peak-to-peak is defined as the difference between the smallest and the largest period sampled during measurement.

Cycle-to-Cycle Jitter (Jcc)

Period Jitter

Peak-to-peak period jitter is the difference between the largest clock period and the smallest clock period for all individual clock periods within an observation window, typically 1,000 or 10,000 cycles. It is a useful specification for guaranteeing the setup and hold time of flip flops in digital systems such as FPGAs.



Period Jitter (J_{per})

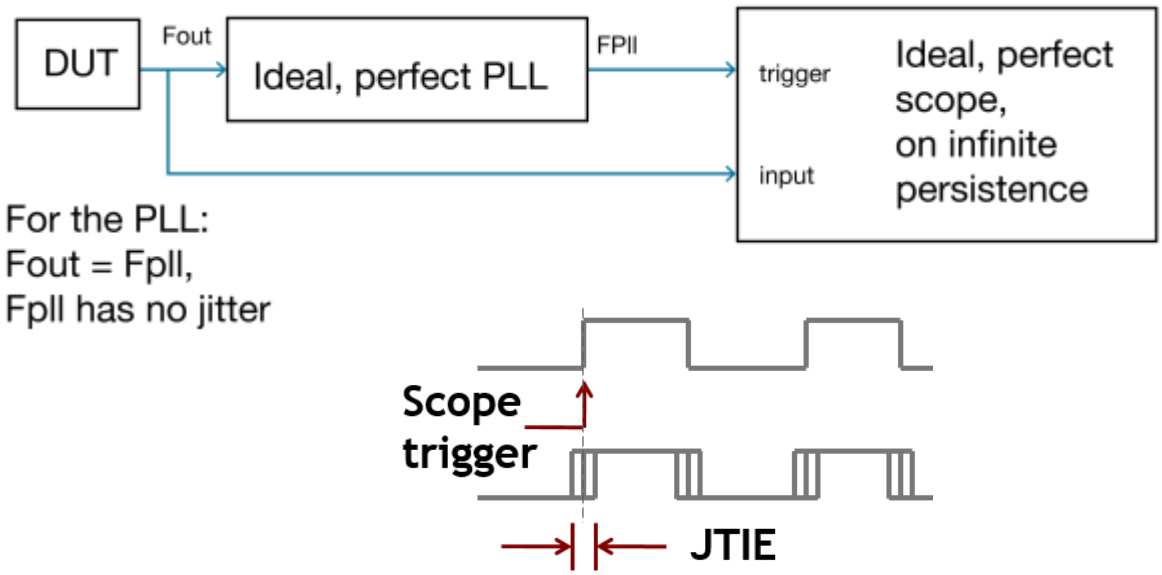
Types of Jitter Measurements

Time Interval Error (TIE) Jitter or Phase Jitter

TIE jitter, also known as accumulated jitter or phase jitter, is the actual deviation from the ideal clock period over all clock periods.

It includes jitter at all jitter modulation frequencies and is commonly used in wide area network timing applications, such as SONET, Synchronous Ethernet (SyncE) and optical transport networking (OTN).

More information on TIE and other jitter types can be found in the Additional Resources section.



TIE Jitter (J_{TIE})

Types of Jitter Measurements

Jitter Measurement Units

Different measurements or statistics can be taken for all types of jitter, although some are more common than others.

Each type of jitter is measured and specified in time increments of the clock error, usually pico-seconds or femto-seconds. A larger number generally indicates a lower performance timing source.

Jitter can also be specified in root mean square (RMS) of the timing increment. Calculating RMS values often assumes a Gaussian distribution and shows the standard deviation (1σ) of the jitter measurement.

RMS Calculation

To calculate the RMS value for "X" where X_{RMS} represents a discrete set of values (X_1 … X_n), use the formula below:

$$X_{RMS} = \sqrt{\frac{1}{n}({X_1}^2 + {X_2}^2 + \cdots + Xn^2)}$$

Time vs. Frequency Domain

Jitter vs. Phase Noise

Jitter is usually a time domain term, while phase noise is a frequency domain term. Although it is common for the terms to be used loosely with the result that they are often used interchangeably.

In theory and with perfect measuring equipment, phase noise measured to an infinite carrier offset would provide the same value as jitter. However, using practical test equipment there will always be a discrepancy between the two.

Furthermore, tools for each measurement provide different views of the same phenomena, which are useful for seeing different types of jitter and frequency anomalies.

Jitter is a time domain term

- Typically measured with an oscilloscope
- Directly measures peak-to-peak and cycle-to-cycle jitter
- Time domain equipment generally has a higher noise floor than frequency domain equipment

Phase noise is a frequency domain term

- Typically measured with a spectrum analyzer in phase noise mode or a phase noise analyzer
- Cannot directly measure peak-to-peak or cycle-to-cycle jitter
- Random jitter vs. deterministic jitter (spurs) are easily recognized
- Spectrum analyzers and phase noise analyzers generally have lower noise floors than time domain equipment
- Can be integrated over different frequency bands to provide RMS phase jitter

Time vs. Frequency Domain Equipment

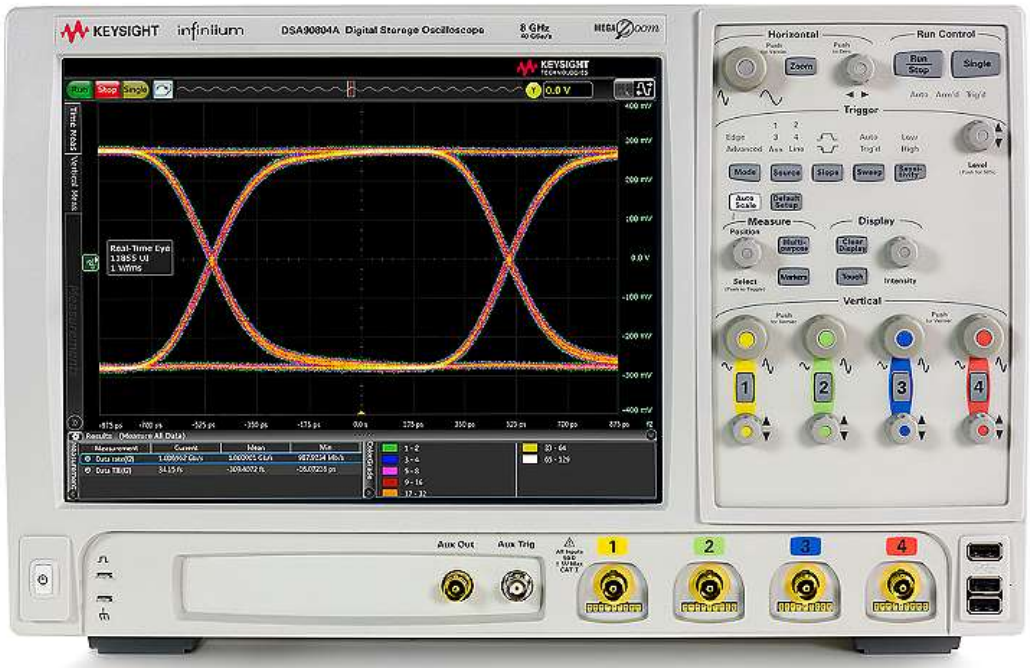
Time Domain Equipment

Time domain equipment is typically a high-speed digitizing oscilloscope.

Only time domain equipment can measure all of the jitter frequency components. It has the virtue of being able to directly measure peak-to-peak, cycle-to-cycle, period and TIE jitter. This measurement approach permits the measurement of jitter of very low frequency clock (or carrier) signals.

By post-processing the data with various techniques such as FFTs and digital filters, it is possible to integrate the phase noise value over a specific band of frequencies to generate RMS phase jitter values.

Time domain equipment is very good at measuring data-dependent jitter, which makes it very useful for high-speed serial links that use serializer/deserializer (SERDES) technology.



Time Domain Equipment Example:
Keysight (Agilent) 90804
Digital Oscilloscope
http://bit.ly/1ENn1hu

Time vs. Frequency Domain Equipment

Frequency Domain Equipment

Frequency domain equipment is usually a spectrum analyzer, a phase noise analyzer or a spectrum analyzer with phase noise measurement capability.

Frequency domain equipment cannot directly measure peak-to-peak, cycle-to-cycle or period jitter because its native capability is to measure the RMS power of signals in a given frequency band. Frequency domain equipment is also awkward for measuring data-dependent jitter.

However, the best frequency domain instruments have a lower noise floor than the best time domain instruments. Spectrum analyzers are also better for recognizing spurs and random jitter.

This fact makes frequency domain instruments the first choice for ultra-low phase noise clock signal measurements.

Frequency Domain Equipment Example:
Keysight (Agilent) E5052B
Spectrum Analyzer
http://bit.ly/1ESzakM

Converting Between Time and Frequency Domain

Converting RMS Jitter (1σ) to Peak-to-Peak

It is often desirable to convert an RMS jitter value to a peak-to-peak number and vice versa. One common approach is to make an approximation using a crest factor and assuming a Gaussian noise model.

A crest factor is calculated for peak-to-peak jitter given an RMS jitter value and a tolerable bit error rate (BER). Once calculated, the resulting crest factor is used to convert between the RMS jitter value and peak-to-peak value.

Conversion Example

Convert RMS jitter (1σ) to / from peak-to-peak jitter
- Most approaches use “crest factors” and are approximations

Peak-to-peak estimate must be based on a specific BER
- Industry typically uses BER = 10^{-12} for clocks

Example conversion
- For BER = 10^{-12}, RMS to peak-to-peak crest factor = 14.069
- So, 1 ps RMS jitter ~= 14.069 ps, peak-to-peak jitter

Generally accepted industry clock BER →

Jitter crest factor (RMS to / from peak-peak)		
BER	Crest factor (α)	+/- StdDev (σ)
1E-11	13.412	6.706
1E-12	**14.069**	**7.034**
1E-13	14.698	7.349

TRY Silicon Labs
Phase Noise to Jitter Calculator

Time vs. Frequency Domain Equipment Summary

	Time Domain Equipment	Frequency Domain Equipment
Native Measurements	• Peak-to-Peak Jitter • Cycle-to-Cycle Jitter • Period Jitter	• RMS Phase Jitter • Phase Noise • Jitter Frequency Information
Advantages	• Good with Low-Frequency Clocks • Good with Data-Dependent Jitter	• Lower Noise Floor • Easy Detection of Spurs vs. Random Jitter

Time vs. Frequency Domain Examples

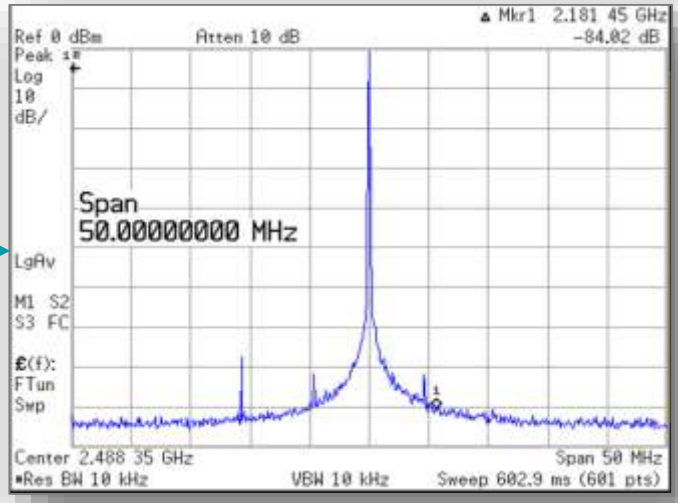
Time Domain Equipment vs. Frequency Domain Equipment

In the following pages, we show time and frequency domain measurements on an oscilloscope and a spectrum analyzer. Both tools show a single sine wave with no modulation, and then with added modulation.

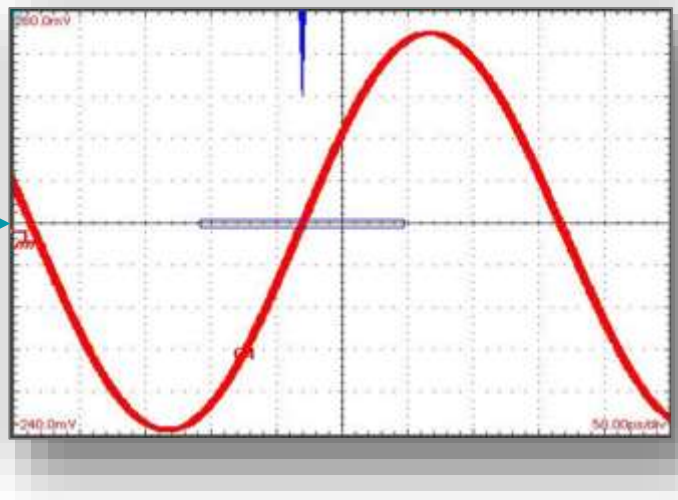
In each plot, jitter is visible and modulation is quite obvious.

2.488 GHz frequency is a common SONET frequency.

Frequency domain plot of 2.488 GHz frequency.

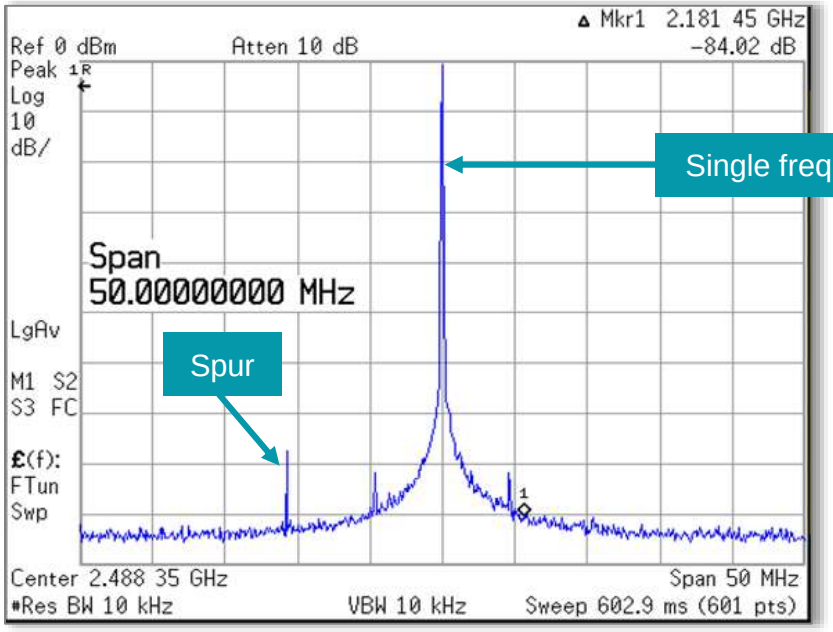


Time domain plot of 2.488 GHz frequency.



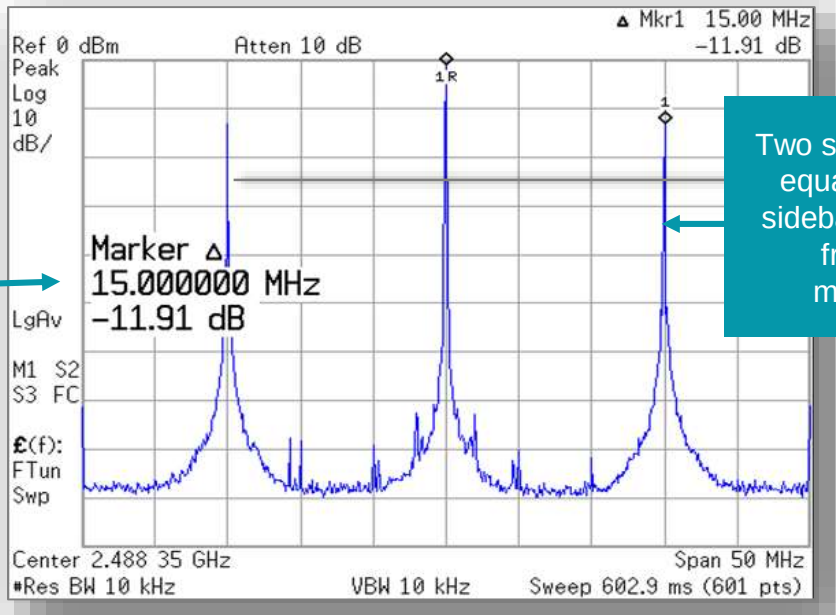
Time vs. Frequency Domain Examples

Frequency Domain: Spectrum Analyzer



2.488 GHz Sine Wave – **Freq Modulation – OFF**

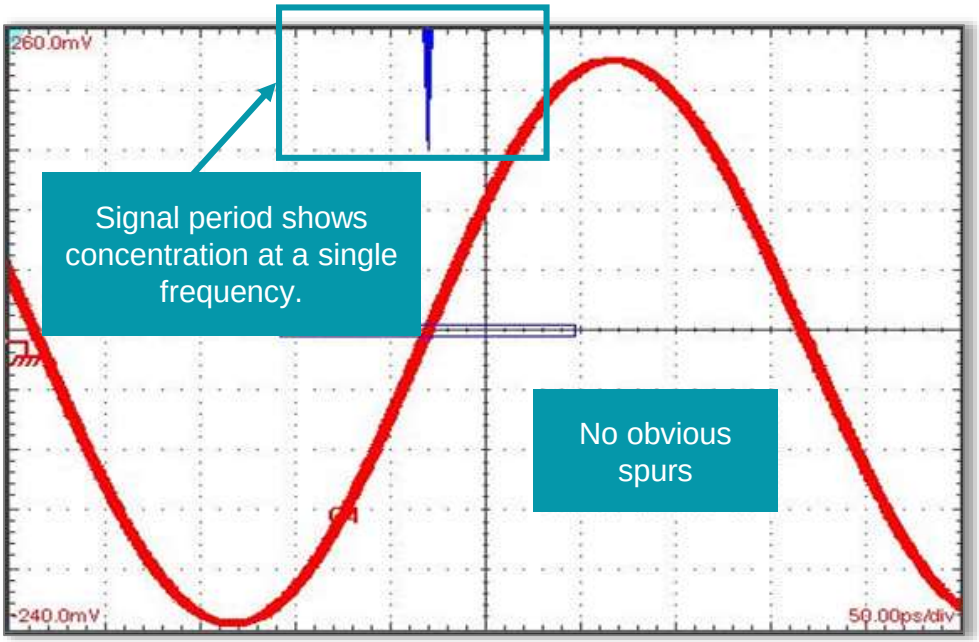
The spectrum analyzer immediately shows the frequency modulation is at 15 MHz.



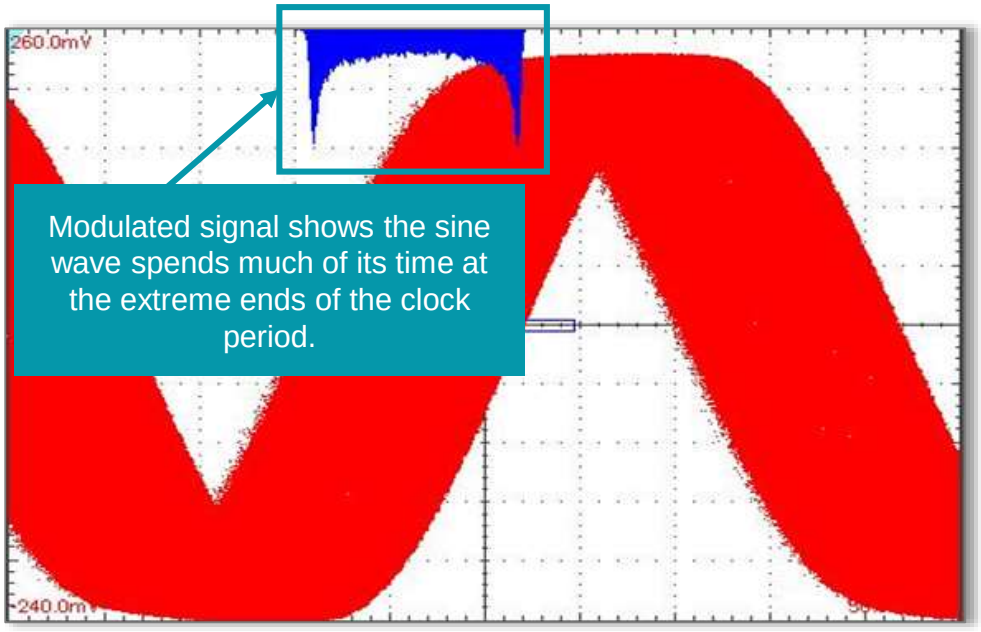
2.488 GHz Sine Wave – **Freq Modulation – ON**

Time vs. Frequency Domain Examples

Time Domain: High-Speed Digitizing Oscilloscope



2.488 GHz Sine Wave – **Freq Modulation – OFF**



2.488 GHz Sine Wave – **Freq Modulation – ON**

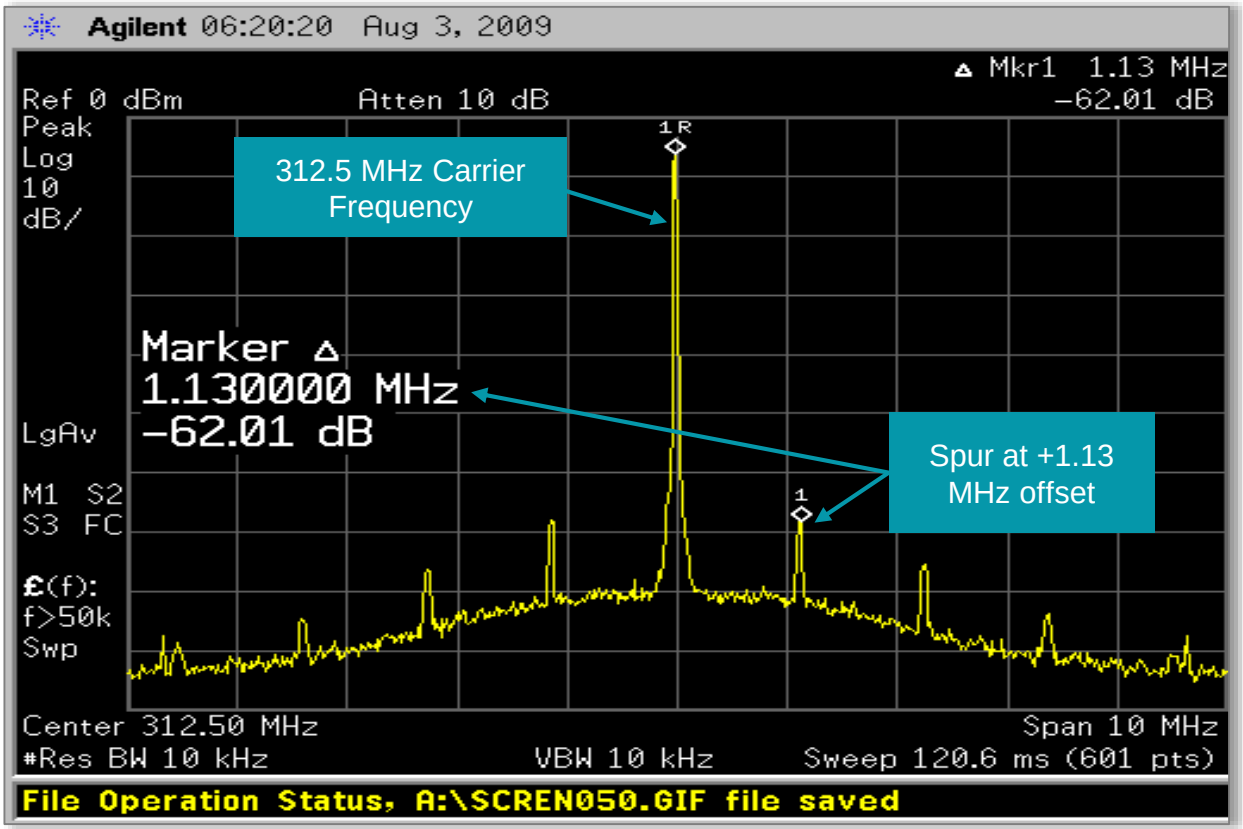
Time vs. Frequency Domain Examples

Frequency Domain: Phase Noise Analyzer, Spectrum Plot

Many applications use phase noise when specifying required maximum clock jitter. Phase noise can be shown in both a frequency spectrum sweep or a phase noise plot, both in frequency domain.

In the frequency spectrum sweep shown below, the plot is mostly symmetric around the Ethernet carrier at 312.5 MHz, with spurs located at both plus and minus offsets.

The marker “1” shows the largest periodic spur at +1.13 MHz positive offset. It also has a mirror spur, roughly the same size and located at the -1.13 MHz negative offset. Mirrored spurs are characteristic of a carrier frequency and accordingly, other spur pairs can be seen.



312.5 MHz Clock Frequency Spectrum Sweep

Time vs. Frequency Domain Examples

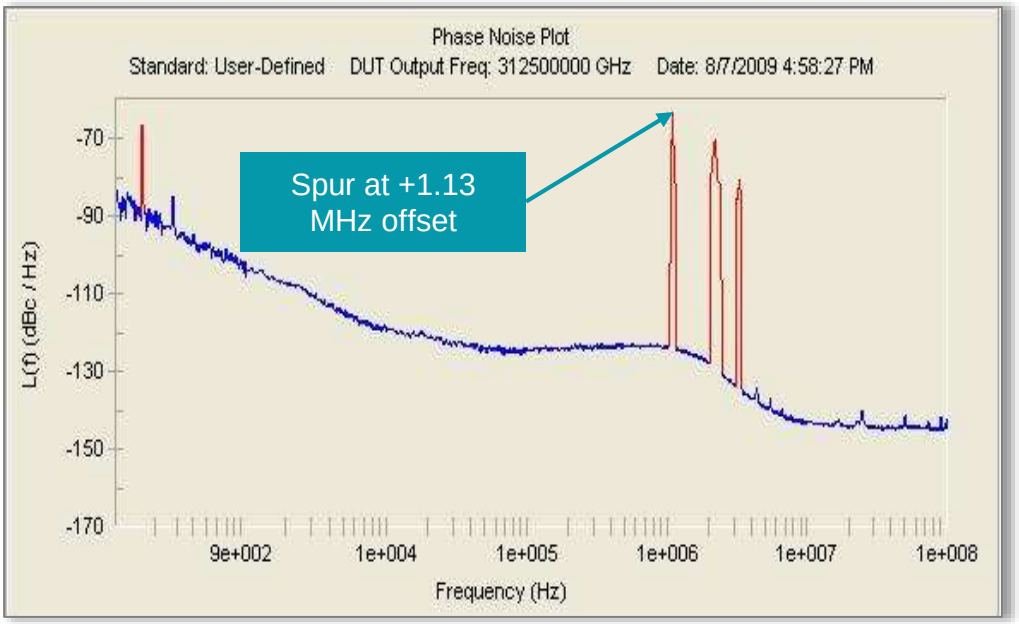
Frequency Domain: Phase Noise Analyzer, Phase Noise Plot

A phase noise plot of the same 312.5 MHz carrier is shown below in a phase noise plot. The carrier does not show up on the plot and is conceptually located to the left of the plot, just off of the *y*-axis.

The phase noise plot shows a “single-sideband,” or only one half of the spectrum. The other half is assumed to be symmetric, as shown in the spectrum sweep on the prior page. The largest spur is again located at +1.13 MHz offset.

Phase noise analyzers calculate RMS noise to include the contribution from the missing half of the spectrum.

Another noteworthy difference between spectrum plots and phase noise plots is that the horizontal scale of phase noise plots is logarithmic while spectrum plots use a linear scale.



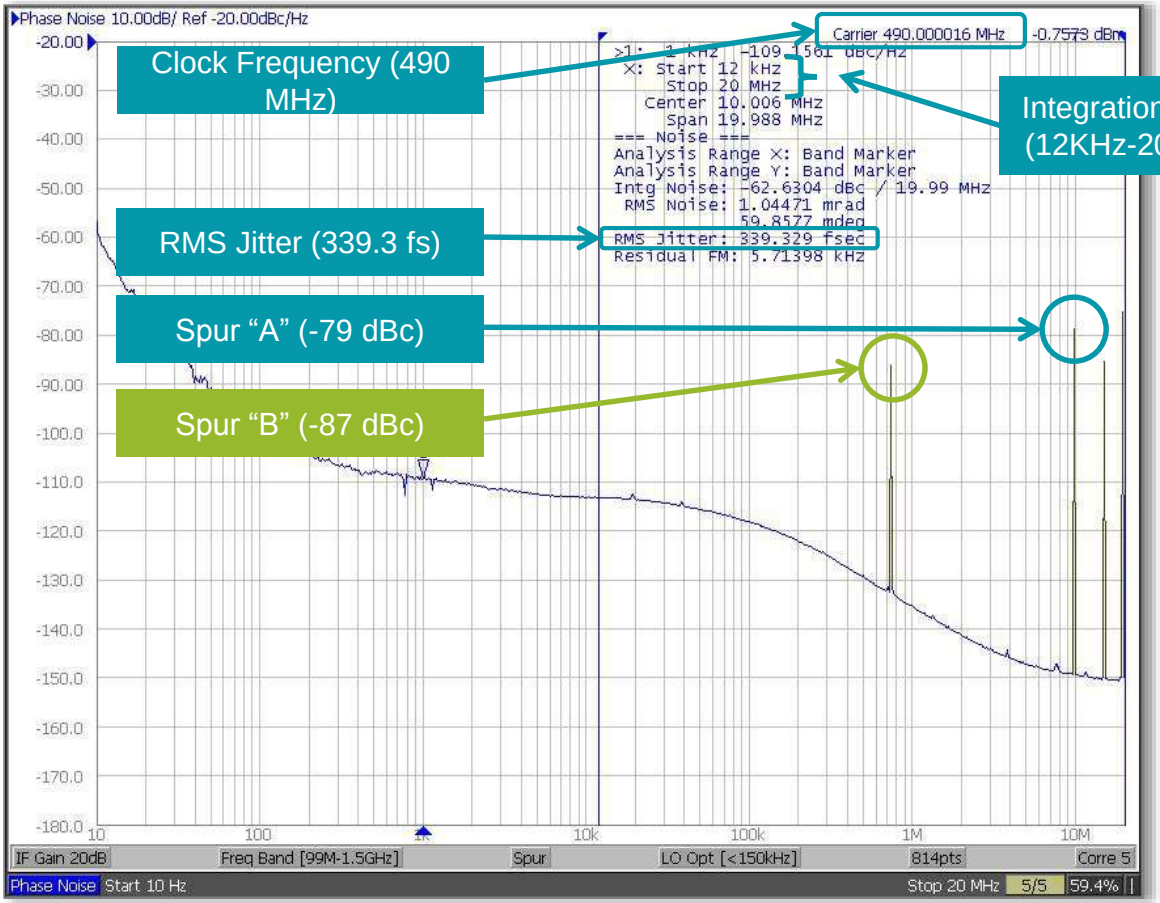
312.5 MHz Clock Phase Noise Plot

Calculating Spur Jitter Contribution

Investigating Spurs

The word “spur” refers to spurious noise. Spurs are periodic and typically stationary. They are also correlated to a noise source.

Spurs are usually modeled as sine wave modulations of the carrier, and they are considered to be jitter at a single offset frequency.



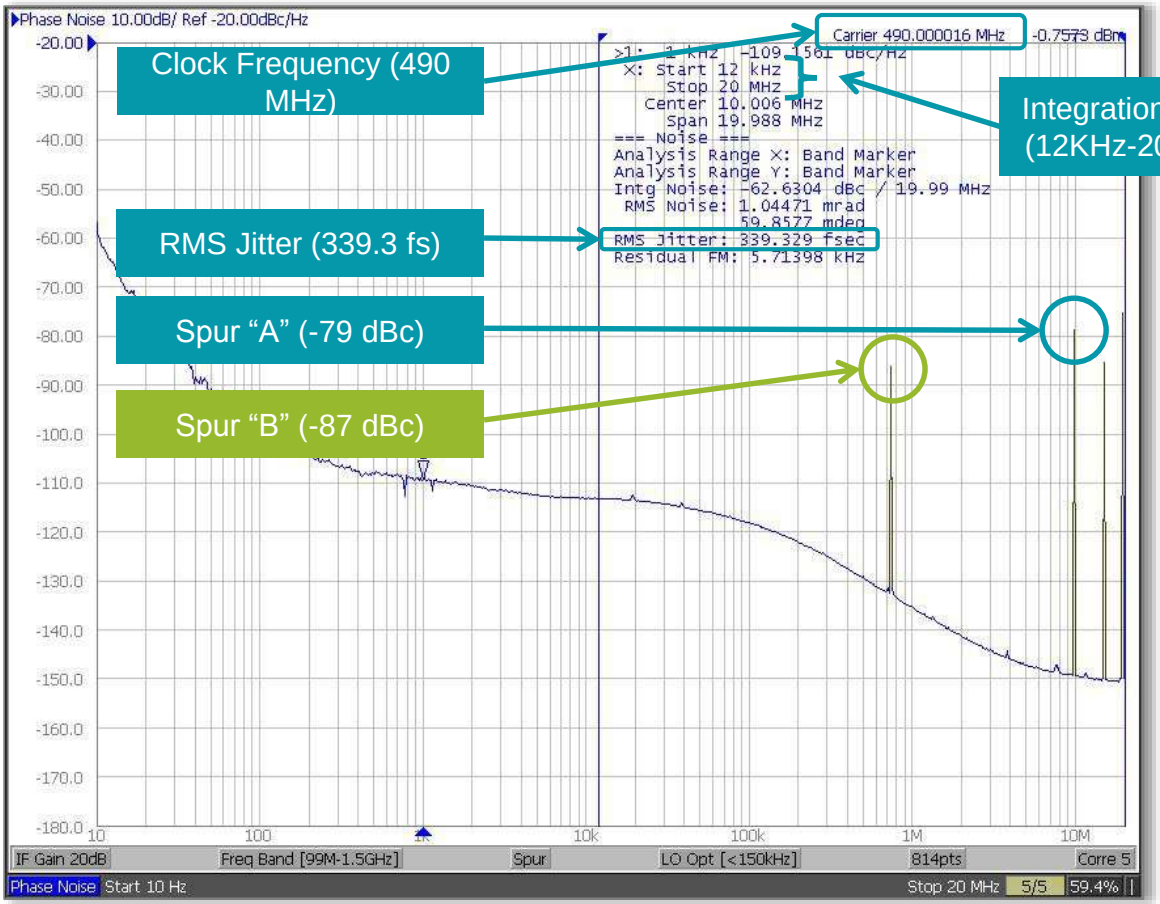
490 MHz Clock Phase Noise Plot

Calculating Spur Jitter Contribution

Characterizing and Calculating Spurs

A spur's jitter contribution is well understood, and typically only large spurs contribute significantly to a system's overall RMS jitter.

- 490 MHz phase noise plot with random Gaussian noise and spurious jitter
- Integration band: 12 kHz to 20 MHz
- Calculated RMS jitter = 339.2 fsec (includes random noise jitter and spurs' jitter)



490 MHz Clock Phase Noise Plot

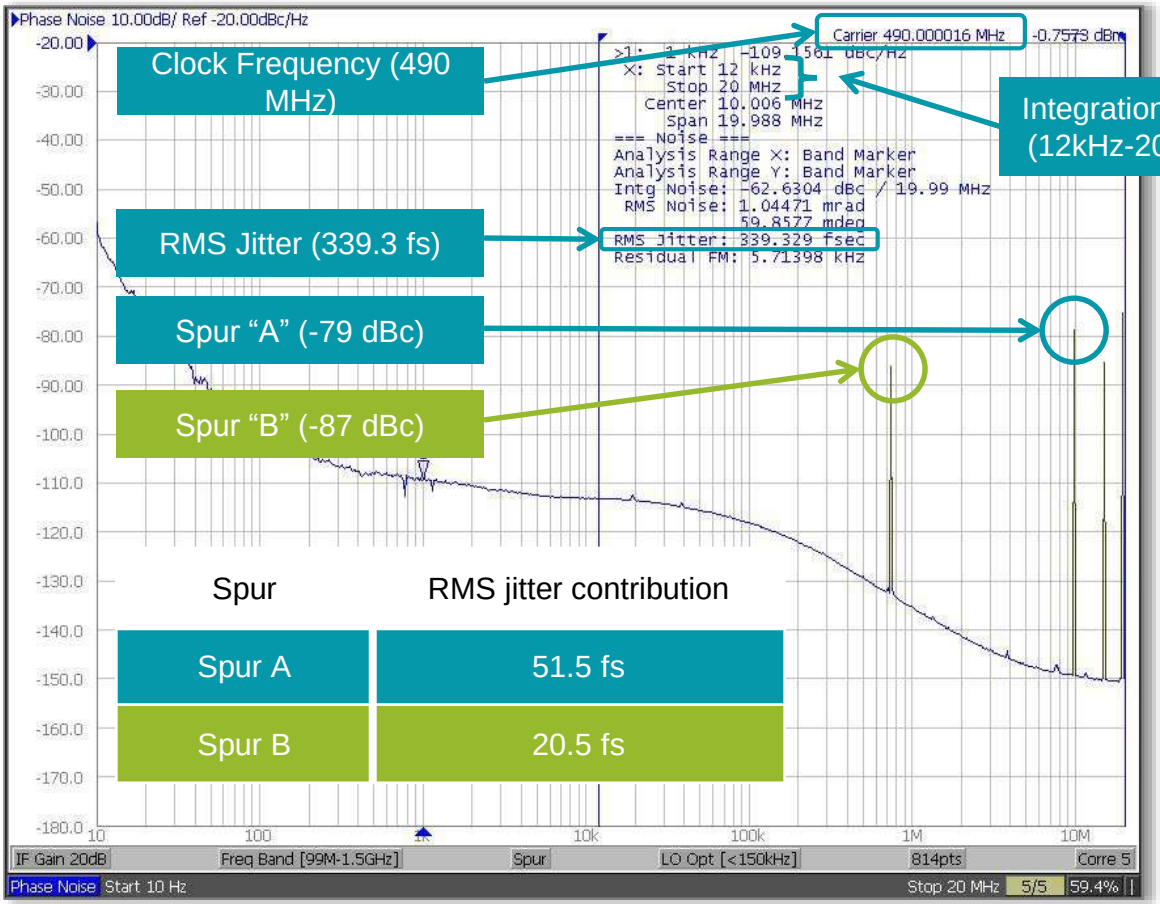
Calculating Spur Jitter Contribution

Characterizing and Calculating Spurs

The following equations shown determine the jitter associated with a spur as shown on a phase noise plot. The required information for this calculation is the carrier frequency and the spur amplitude in dBc.

$$\boldsymbol{Jitter_{pk-to-pk}} = \left(\frac{2}{\pi} \cdot 10^{\frac{S}{20}}\right) \cdot \left(\frac{1}{F}\right) \text{ -- AND -- } \boldsymbol{Jitter_{RMS}} = \frac{Jitter_{pk-to-pk}}{2\sqrt{2}}$$

Where, S = spur amplitude in dBc, F = clock (carrier) frequency in Hz



Spur	RMS jitter contribution
Spur A	51.5 fs
Spur B	20.5 fs

490 MHz Clock Phase Noise Plot

Calculating Spur Jitter Contribution

How Do Spurs Affect Total RMS Jitter?

RMS values “add” using the Root Sum Square (RSS) equation. In other words, to calculate a total RMS of separate RMS values, take the square root of the sum of the square of each value.

Quantifying the jitter contribution of spur A & B, we use the RSS equation to “back out” each spur’s RMS jitter from total RMS jitter, arriving at the RMS jitter without the spurs.

- $J_{total(RMS)}$ = 339.3 fs (from screen capture)
- $J_{spurA(RMS)}$ = 51.5 fs (from calculation)
- $J_{spurB(RMS)}$ = 20.5 fs (from calculation)
- $339.3\text{fs} = \sqrt{J_{noAB(RMS)}{}^2 + J_{spurA\,(RMS)}{}^2 + J_{spurB\,(RMS)}{}^2}$
- $339.3\text{fs} = \sqrt{J_{noAB(RMS)}{}^2 + 51.5\text{fs}^2 + 20.5\text{fs}^2}$
- $J_{noAB(RMS)} = \sqrt{J_{total(RMS)}{}^2 - J_{spurA\,(RMS)}{}^2 - J_{spurB\,(RMS)}{}^2}$
- $J_{noAB(RMS)} = \sqrt{339.3\text{fs}^2 - 51.5\text{fs}^2 - 20.5\text{fs}^2}$
- $J_{noAB(RMS)}$ = 334.7 fs

Summary

- Total RMS jitter (including spurs) = 339.3 fs
- Removing spur A & B contribution leaves RMS jitter = 334.7 fs
- Result: spurs A & B are small contributor to total RMS jitter.

Summary

Jitter falls into two categories: random and deterministic. Random jitter is unbounded and hard to diagnose.

Deterministic jitter is often periodic and narrowband. It is also often correlated to a particular noise generator. More than one noise generator can create jitter that may appear uncorrelated on clock output signals.

Different applications rely on different measures of jitter. The most comprehensive measurement is TIE or phase jitter, and requires an ideal clock to compare the tested clock against. Period jitter and cycle-to-cycle jitter compare the clock to itself to identify variations within the clock cycles.

Jitter is measured in the time or frequency domain by different types of equipment. Time domain equipment generally has a higher noise floor than frequency domain equipment. Time domain equipment effectively presents period and cycle-to-cycle measurements. Frequency domain equipment effectively shows deterministic jitter (spurs) and random jitter.

Spurs contribute to overall jitter, and can be measured and accumulated via equations provided.

Silicon Labs timing technology and expertise reduce jitter and speed time to market.

Silicon Labs Timing Solutions

This tutorial focuses on various types of jitter and how to measure them.

Silicon Labs provides expertise, tools and solutions for how to quantify, identify and eliminate jitter from systems.

Our timing solutions are all customizable for any frequency and any output and deliverable in less than two weeks.

Go to Clocks

Ultra-low jitter any-frequency, any-output, single-chip clocks, jitter attenuators, and network synchronizers.

Go to Buffers

Ultra-low jitter universal clock buffers and level-translators for any format and any voltage.

Go to Oscillators

Ultra-low jitter any-frequency, any-format oscillators.

Try the Silicon Labs
Phase Noise to Jitter Calculator

Thank You

www.silabs.com/timing

Additional Resources

- AN279 – Estimating Period Jitter from Phase Noise – This application note reviews how RMS period jitter may be estimated from phase noise data. This approach is useful for estimating period jitter when sufficiently accurate time domain instruments, such as jitter measuring oscilloscopes or Time Interval Analyzers (TIAs), are unavailable.
- AN491 – Power Supply Rejection for Low-Jitter Clocks – Hardware designers are routinely challenged to increase functional density while shrinking the overall PCB footprint. One significant challenge is minimizing clock jitter. Since noise and interference are everywhere and since multiple components share a common power supply, the power supply is a direct path for noise and interference to impact the jitter performance of each device. Therefore, achieving the lowest clocking jitter requires careful management of the power supply.
- AN687 – A Primer on Jitter, Jitter Measurement, and Phase-Locked Loops – This primer provides an overview of jitter, offers practical assistance in making jitter measurements and examines the role phase-locked loops have in this field.

Glossary

- Stochastic process - https://en.wikipedia.org/wiki/Stochastic_process - In probability theory, a stochastic (/stoʊˈkæstɪk/) process, or often random process, is a collection of random variables, representing the evolution of some system of random values over time. This is the probabilistic counterpart to a deterministic process (or deterministic system). Instead of describing a process that can only evolve in one way (as in the case, for example, of solutions of an ordinary differential equation), in a stochastic or random process there is some indeterminacy; even if the initial condition (or starting point) is known, there are several (often infinitely many) directions in which the process may evolve.
- Aperiodic - http://www.merriam-webster.com/dictionary/aperiodic - of irregular occurrence; not periodic.
- FPGA - https://en.wikipedia.org/wiki/Field-programmable_gate_array - A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer after manufacturing – hence "field-programmable."
- Crest factor - https://en.wikipedia.org/wiki/Crest_factor - Crest factor is the ratio of peak value to the rms value of a current waveform.

Author

James Wilson, Marketing Director, Timing Products

James Wilson is the director of marketing for Silicon Labs' timing products, managing product strategy, roadmap development, new product initiatives, product management, software development and marketing promotions. As part of his role, Mr. Wilson has been a key contributor in architecting Silicon Labs' online strategy to offer mass-customized clocks and oscillators using simple web-based tools. Prior to joining Silicon Labs in 2002, Mr. Wilson held a variety of marketing, product management and engineering roles at Freescale and various start-ups. Mr. Wilson holds a Bachelor of Science degree in mechanical engineering and a master's degree in business administration from the University of Texas at Austin.