

100V Surge Stopper Protects Components from 300V Transients

Hamza Salman Afzal

High voltage transients in automotive and industrial systems are common and can last from microseconds to hundreds of milliseconds, sending significant energy downstream. Transient causes include automotive load dumps, and spikes caused by load steps and parasitic inductance. To avoid the risk of failure, all electronics in these systems must either be robust enough to directly withstand the transient energy spikes, or they must be protected from them.

The LT4356 surge stopper is a dramatic performance upgrade over traditional, passive clamp protection techniques. It actively protects downstream components from overvoltage by regulating the gate of a pass MOSFET and it limits current with the help of a standard sense resistor. Figure 1 shows a typical 12V application.

The LT4356 has a rated maximum of 100V with an operating voltage range of 4V to 80V, making it ideal for protecting downstream electronics in a wide variety of industrial and automotive applications. Nevertheless, some circuits require protection against transients as high as 200V to 300V.

Figure 2 shows one way that the LT4356 can be made to suppress such high voltages, but at the cost of the current limiting feature. In Figure 2 the V_{CC} and SNS pins are decoupled from the raw input voltage and separately clamped to a safe value below 100V. Since the V_{CC} and SNS pins are of necessity disconnected from the input path, current sensing is not possible and the circuit serves only as a voltage clamp.

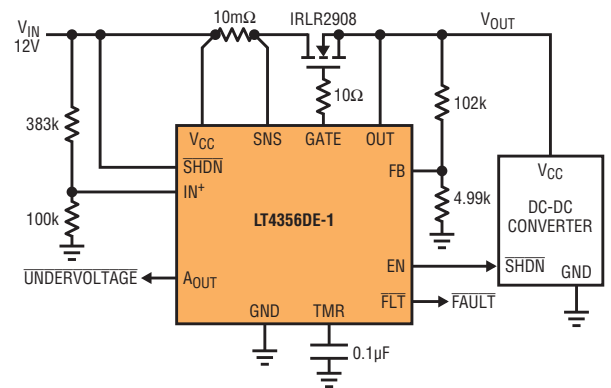


Figure 1. 12V overvoltage regulator

It is possible to overcome this limitation by cascading a second pre-regulating MOSFET, Q2, as shown in Figure 3. Q2 clamps the V_{CC} and SNS pins to a safe level, restores the current limit feature and as an added benefit, shares SOA (safe operating area) stress with Q1.

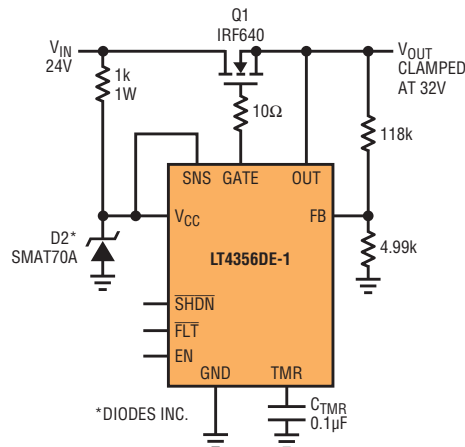
When power is first applied, R3 and D1 pull up on the gate of Q2, which in turn passes power through to the LT4356. The GATE pin then pumps up the gates of Q1 and Q2, fully enhancing both MOSFETS

and sending power through to the output. Thus R3 and D1 are critical to start-up. Under normal operating conditions the GATE pin limits itself to about 12.5V above the output, so with 12V at the input, Q1's gate is biased to 24.5V and Q2's gate is biased slightly lower, about 24V.

When the input is subjected to a high voltage transient, R3 and D1 pull up on the gate of Q2, which in turn is clamped by D2 to approximately 80V. Acting as a source follower, Q2's source rises no further than about 75V, keeping V_{CC} and SNS safely below their 100V maximum rating. Unlike the shunt clamped application shown in Figure 2, the series clamped topology of Figure 3 permits full use of the LT4356's current limiting feature. Q1 regulates in the normal way, limiting the output voltage as prescribed by R1 and R2.

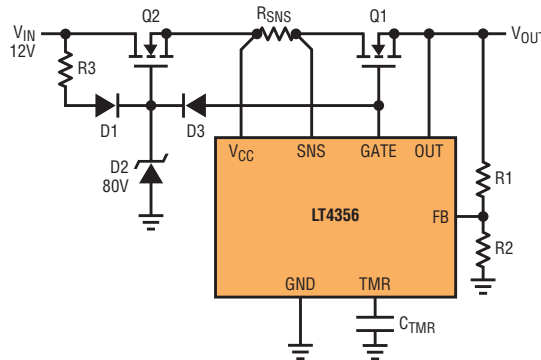
An added benefit of the topology shown in Figure 3 is that Q2 shares SOA stress with Q1. For inputs in the range of 150V to 200V, the SOA stress is shared equally between Q1 and Q2. In certain applications this allows two inexpensive

Figure 2. 24V application circuit capable of withstanding 150V



The LT4356 has a rated maximum of 100V with an operating voltage range of 4V to 80V, but a little extra circuitry enables it to protect against transients as high as 300V.

Figure 3. Pre-regulator topology extends protection range of the LT4356. Figure 4 shows the complete circuit.



to recognize the potential for high dv/dt at the input and resulting consequences. Until the circuit can respond, current arising from an instantaneously applied high input voltage is limited only by the parasitic inductance and the path resistance to the output capacitor. While most test waveforms specify some sufferable rise time, an infinite input slew rate is not inconceivable, such as might arise during bench testing. Q3 is added to give the LT4356's current limit loop a head start under these conditions.

MOSFETs to replace a single, and much more costly, special high SOA device. As the peak input voltage requirement rises above 200V, the SOA becomes increasingly concentrated in Q2 and the series connection offers no substantial relief.

described, Q2's gate is clamped at 80V so that with a 300V input, Q2 drops 225V, while Q1 sees no more than 75V total. For this reason a 250V device is specified for Q2, and a 100V device suffices for Q1. It is possible to withstand even higher input voltages by appropriate selection of Q2.

Figure 5 shows the results of the circuit subjected to a 300V spike. C_{TMR} is sized to ride through such excursions, but longer duration surges will be interrupted, thereby protecting the MOSFETs from certain destruction. ■

Figure 4 shows a complete circuit based on the new topology, designed to withstand up to 300V peak input. As previously

When designing circuits to withstand such high input voltages, it is important

Figure 4. 16V overvoltage regulator capable of blocking 300V transients

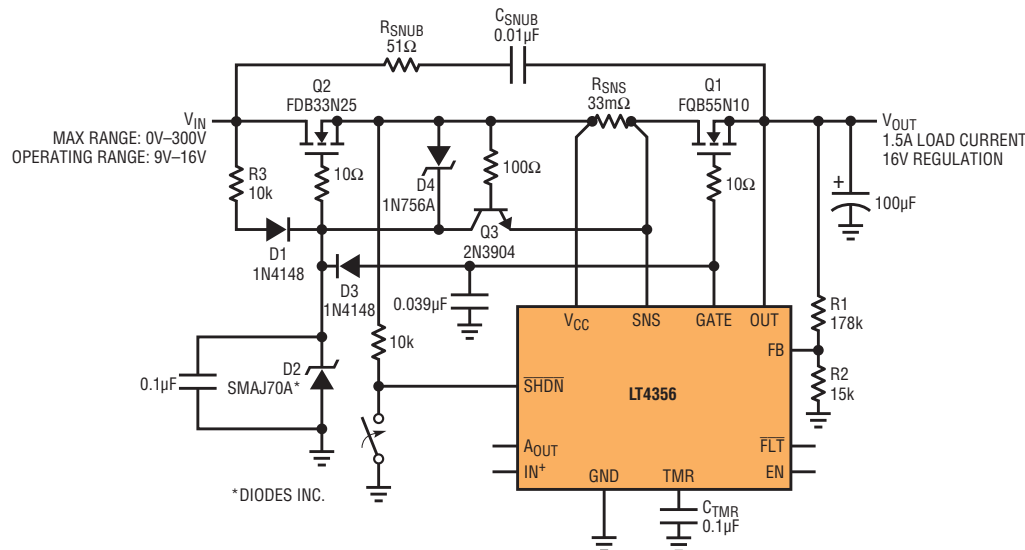


Figure 5. Results of 300V spike on input of circuit in Figure 4

