

Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

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Monolithic sigma-delta converters with 21-bit resolution (page 8)

SPICE macromodel of an analog multiplier (page 18)

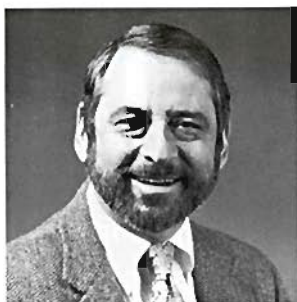
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Editor's Notes

FAREWELL, PHILBRICK

About one mile (as the crow flies) from where these words are being written, there is a plant bearing a soon-to-disappear 'Teledyne Components' designation. The plant was built in the early '60s to house George A. Philbrick Researches, Inc., at the height of its prosperity; and from 1967 until recently it bore the name Teledyne Philbrick.



The company was incorporated in 1946 by the late George Philbrick, about ten years after he had built the first electronic analog computer (or as he spelled it, *computer*). Then, 40 years ago (1952), he offered to a barely comprehending world the first general-purpose differential operational amplifier, Model K2-W.

The K2-W, the heart of the analog computer, was a striking-looking octal-based plastic plugin with two 12AX7 tubes sticking out the top (see *Analog Dialogue* 16-3, p. 2). It was originally intended to allow engineers to design and build special-purpose analog computers cheaply, but within five years, it—with its successors—became the tail that wagged the dog, the harbinger of a whole new analog measurement-, control-, and signal-processing industry—heralded by Philbrick's publications, products, and people. Now, as Philbrick fades into the mists of history, it behooves us in the industry (and those we serve) to recognize our debt of gratitude and salute this pioneering firm.

BARRIE GILBERT HONORED BY IEEE

We are pleased to note that Analog Devices Fellow—and IEEE Fellow—Barrie Gilbert has received the 1992 IEEE Solid-State Circuits Award "for contributions to non-linear analog signal processing circuits." The award, established in 1987, is sponsored by the IEEE Solid-State Circuits Council for outstanding contributions in the field of solid-state circuits. Earlier recipients included James D. Meindl, Toshiaki Masuhara, and Frank Wanlass.



CORRECTION

In *Analog Dialogue* 25-2, page 23, in an article announcing the naming of two new Analog Devices Fellows, we published what purported to be an up-to-date list of Fellows. Unfortunately, Fred Mapplebeck's name was inadvertently omitted—for which we apologize. Carl Roberts, recently named a Fellow, will be covered in the next issue. The list now looks like this:

- | | |
|---------------------------|-------------------------|
| Derek Bowers (1991) | A. Paul Brokaw (1980) |
| Lew Counts (1984) | Barrie Gilbert (1980) |
| Jody Lapham (1988) | Fred Mapplebeck (1989) |
| Jack Memishian (1980) | Wyn Palmer (1991) |
| Carl Roberts (1992) | Michael P. Timko (1982) |
| Robert W. K. Tsang (1988) | Mike Tuthill (1988) |

Dan Sheingold

THE AUTHORS

David Whitney (page 10), who designed the AD811, is a design engineer in the Amplifier Group at Analog Devices Semiconductor. For most of his eleven years at Analog, Dave was a Product Engineer, working on such products as the low-noise AD712 op amp family and the high-speed AD840 series. He received his BSEE in 1981 from Northeastern University, where he is currently working on an MSEE.



John O'Connell (page 7) is a Product Marketing Engineer at Analog Devices BV, Limerick, Ireland, for industrial-control, converter-, and switch/mux products—and regionally for France and Germany. He has worked in Quality Assurance and Test Engineering and has a BS in Engineering—Electronics and an MBA. His interests include swimming, golf, flying, and badminton.



Walt Jung (page 14) is a Corporate Staff Applications Engineer at ADI. Earlier, he consulted on application projects and he has written a variety of application notes and articles that appeared in *Analog Dialogue* and the trade press. He has authored books (*IC Op Amp Cookbook*) and many articles on linear IC applications. Walt attended Drexel Institute of Technology, is a member of IEEE and a Fellow of the AES. He enjoys live and recorded music.



Bill Schweber (page 3) is a Senior Technical Marketing Engineer and Contributing Editor to *Analog Dialogue*. Besides having his BSEE and MSEE degrees, he has designed μ P-based machine controls, been a product marketing engineer, and written three textbooks. He contributes numerous articles to *Analog Dialogue* and the electronics press—many of which introduce new products to the market.



(More Authors on page 22)

The cover illustration is an adaptation by Shelley Cohane of a worldscape from IMTEK IMAGING/MASTERFILE.

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IF Stages Are Going Digital for both Analog and Digital Signals

Monolithic I/O chips provide critical functions for GSM and TIA communications

by Bill Schweber

For many years after Maj. E.H. Armstrong conceived the superheterodyne receiver architecture in the early decades of this century, the critical intermediate stage (IF) and the subsequent detection stage have been analog circuit functions. But with the increasing power and flexibility of digital circuitry—accompanied by faster, higher-resolution converters—even these stages are being implemented digitally, for both analog and digital signals.

THE TRADITIONAL SUPERHET

In a basic single-conversion superheterodyne receiver, the incoming radio-frequency (r-f) signal may be amplified, is then mixed with (i.e., modulated by) a local-oscillator (LO) signal, generated within the receiver. This LO frequency is designed to automatically track the carrier frequency as it is tuned, maintaining a constant offset from carrier, such as 455 kHz or 10.7 MHz. The resulting signal contains sum and difference frequencies at the (carrier \pm LO) values. The next stage, narrowly tuned to the (constant) difference frequency, or *intermediate* frequency (IF), filters out the sum signal and any harmonics.

The great virtue of this *heterodyning* lies in the fact that the LO is tuned at a fixed offset frequency from the carrier, as it is tuned, so that the IF is fixed. Therefore all IF circuitry can be optimized to work around a single, known frequency, and many circuit parameters that normally vary with frequency—such as the properties of high-frequency coupling transformers—remain constant, regardless of the *carrier* frequency being tuned.

For higher performance, *double-conversion* superhets are used when relatively high-frequency carriers (>100 MHz) must be tuned with narrow bandwidth (say 10 kHz). The double-conversion superhet (Figure 1) has a tunable first IF stage, which down-converts the carrier to a mid-range IF (such as 70 MHz); then a fixed LO mixes this IF to a lower IF for additional gain; and the result, which may be also used to derive an automatic-gain-control (AGC) signal, is demodulated to baseband.

The double conversion superhet requires more circuitry than a single-conversion version, but performance is potentially much better. The fixed LO is a much less demanding design, and its use permits an optimal design for a high-stability first LO.

The final stage can be considered an analog signal processor. The last IF output is amplified, demodulated, and filtered to recreate the original modulating signal—an analog or digital waveform—that was impressed on the carrier at the transmitter (AM, FM, SSB, or CW). The IF performance is unaffected by the meaning or coding of the modulating waveform; that information is extracted and processed by the chosen demodulator circuitry.



DIGITAL IF STAGES

The digital IF stage replaces the demodulation circuitry with an appropriate high-speed a/d converter (ADC), digital signal-processor (DSP), and d/a converter(s). The transformation from IF to baseband frequency is made by deliberately undersampling

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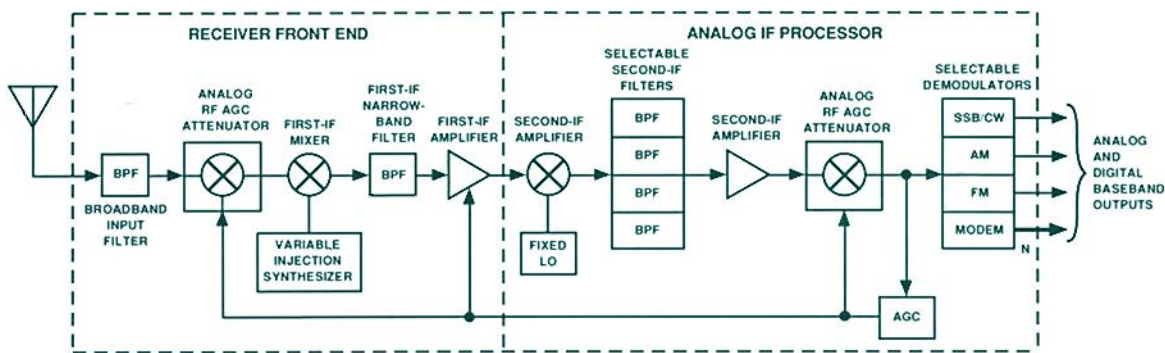


Figure 1. Traditional analog superheterodyne receiver.

the IF signal at a sampling rate that produces an alias at baseband—and filtering out all other aliases (Ref. 4).

According to the Nyquist theorem, sampling at a rate two or more times the bandwidth of a signal completely captures all the information content of the signal. This does not mean that the sampling must always be at least $2 \times$ a signal's highest frequency—only the highest frequency of the *baseband signal*. If the signal is modulated onto a much-higher-frequency RF or IF carrier, the carrier frequency does not affect the Nyquist requirement. Indeed, the Nyquist theorem is used to facilitate detection, since an appropriately chosen undersampling rate (sampled at less than twice the carrier) can produce an alias at baseband, which includes all the required signal information.

If this is so easy, why hasn't it been done more often? First, to be usable, the digitized signal usually needs further processing involving DSP techniques and/or high-performance d/a converters in conjunction with analog circuitry. Second, although the a/d converter need only be sampled at the Nyquist rate, the converter must have sufficient bandwidth to handle the carrier (or IF) frequency. This is challenging when the IF is at several megahertz and above; but devices are available to meet the challenge. For example, the AD770 monolithic a/d converter, which has a 250-MHz bandwidth, can sample at up to 200 MSPS.

I AND Q CHANNELS

The simplest way to impress binary information on a carrier is to directly modulate it, using AM or FM. This provides a direct relationship between the raw data stream and the resulting modulation. It also provides the greatest noise immunity, since the levels embodying logic 1s and logic 0s are widely separated.

Unfortunately, this approach makes inefficient use of available channel bandwidth. For better use of the bandwidth and to transmit more information, the binary data is encoded to modulate the carrier using a subdivided amplitude range: 4, 8, 16, 32, or even more levels. But lessening the amplitude between modulated signal states causes the probability of error to increase. [The logical continuation, to the infinite number of possible levels in a purely analog signal, makes most efficient use of the channel bandwidth but provides the least noise immunity.]

In a technique to create a pseudo-analog signal that improves the transmission of binary information in the presence of noise, the digital data is encoded into two streams. One modulates an in-phase carrier ("I"); the other modulates a 90°-shifted (quadrature, or "Q") carrier. The I and Q signals are added to produce the final transmitted signal. In the traditional analog receiver, the I and Q components are demodulated separately, using two-phase detection. Next, the signals are processed to recover the I and Q data and decode them, recreating the original binary bit stream.

DIGITAL IF PROCESSING

Digital IF processing replaces conventional demodulation by digitizing the IF signal, digitally recreating and processing the I and Q channels, and using digital signal processing to reproduce the sampled AM, FM, CW, SSB, and data signals. D/A converters and anti-imaging low-pass filters then recreate the original modulating waveforms. Since the processor can be programmed for differing filter configurations and parameters, the same circuitry can be used for many modulation techniques and coding algorithms, adapting to differing channel conditions.

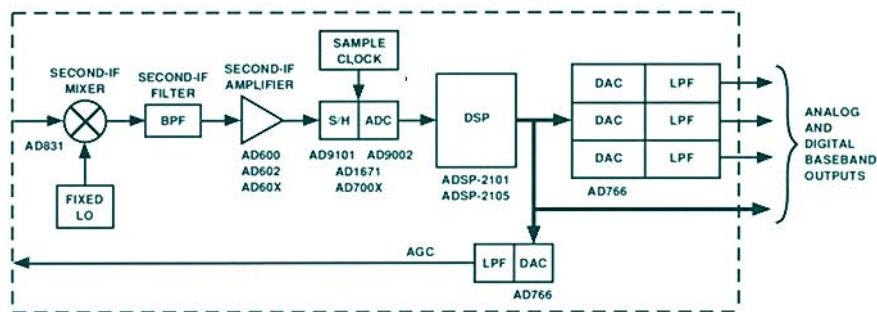


Figure 2. Digital IF processor and detector, showing representative mixed-signal chips.

DIGITAL CELLULAR PHONE

Today's cellular phones use a pair of analog channels for voice and a pair of digital channels for phone/baseband information and control signals (Ref. 1). To increase the number of users that the available assigned spectrum can support, next-generation phones will use all-digital channels (2). These cellular phones digitize and encode the user's voice, to reduce bandwidth requirements and allow time-division multiplexing of independent users. Undersampling is used for IF to baseband demodulation (3).

The specification for such phones, referred to generically as digital mobile radio (DMR), is known in Europe as *Groupe Speciale Mobile* (GSM). The North American version is known as the Telecommunications Industry Association (TIA) standard.

Figure A shows how each 200 kHz of channel spectrum contains data from eight users. Each user is assigned a time slot of 0.577 ms, during which a burst of 156 bits is transmitted at a modulation frequency of approximately 270 kHz.

The overall GSM phone (Figure B) requires an a/d and a/d/a converter for voice conversion; it uses sophisticated algorithms for data compression (encoding) and decompression (decoding) to significantly reduce the overall bit rate. The data stream also

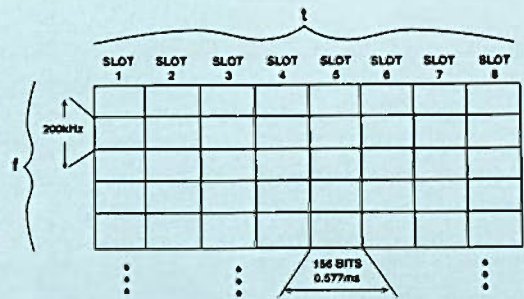


Figure A. GSM time and frequency allocations.

has error-detection and -correction bits appended, to increase coding robustness and minimize overall performance degradation as the SNR decreases.

To achieve this, a GSM phone incorporates a mixed-signal processor, e.g., the Analog Devices ADSP-21msp50, for converting the voice signals, real-time execution of the algorithms, tone generation and detection, signalling, and overall phone management. The DSP works in close coupling with a baseband I/O port, such as the AD7002 (Figure C), to provide the transformation from digitized and compressed baseband audio to the IF stage (for *transmit*) and from IF stage to back to baseband (for *receive*).

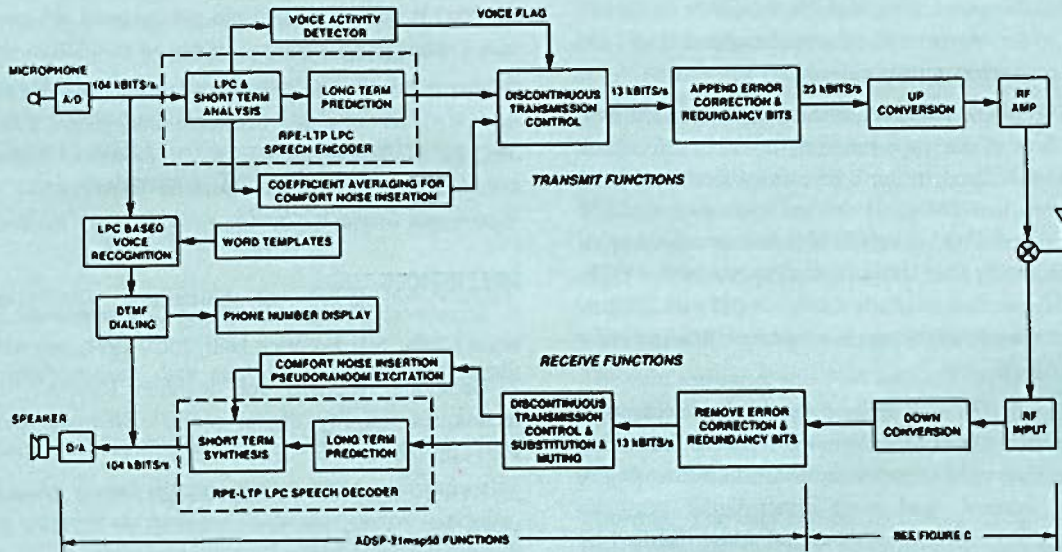


Figure B. GSM phone—overall block diagram.

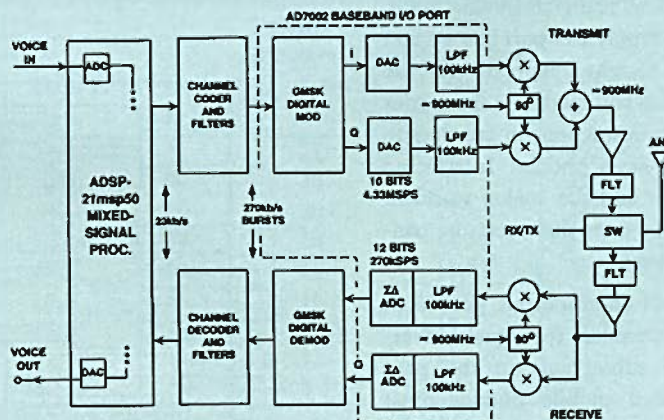


Figure C. GSM baseband I/O functions (up- and down-conversion).

Of course, there are *caveats*. Besides the need for adequate speed and flexibility in the DSP, the performance of the ADC that does this "baseband" conversion is critical. Overall specs—distortion, SNR, BER, and other common measures—can be degraded by a converter with inadequate linearity and dynamic range. Converters with inadequate differential nonlinearity may require dither injection to improve low-level performance.

OTHER CONSIDERATIONS

The sampling rate limits how much real-time processing a given DSP can perform on each sample. Thus, the DSP designer wants to use as low an IF and sample rate as possible, while the analog front-end designer wants a high IF and sample rate to control images and aliasing in the a/d converter—and avoid a sophisticated first-IF filter. This tradeoff is resolved by careful selection of the s/h and a/d circuitry, using components which are characterized for full-linear bandwidth at the carrier frequency.

In an all-analog design, it is easy to add gain in all IF stages, including the second IF. But in a digital IF design, all of the gain must occur before the a/d conversion; and enough front-end gain must be provided to drive the a/d converter adequately without overdriving it. With too much gain, undesired out-of-band signals can pass through the wider-bandwidth receiver front end and saturate the A/D. Such A/D saturation generates aliased in-band harmonic- and intermodulation-distortion products which can block weak signals. To avoid this, high-performance automatic gain control (AGC), derived from the digital baseband level, and low-distortion a/d converters must be used.

AGC is not unique to digital receivers, of course. It has been used since the earliest days of the superheterodyne—it is a feedback loop that uses received signal strength to control front-end gain. In an analog receiver, the feedback is derived from the second-IF level; but in a digital receiver, the AGC signal is usually derived from the narrow-band IF filter output (implemented by a DSP) and converted back to analog to adjust the front-end gain. Digital feedback may also be used, effecting a sort of block floating-point adjustment to the digital level.

The trend today in selected well-defined applications with well-understood characteristics is toward digital IF. Just as the tuning function in most receivers has migrated from continuous analog to synthesized digital control, and even direct-digital synthesis (DDS), the IF stage is moving towards digital when justified by cost, complexity, or performance requirements.

Among the first mass-market applications is digital mobile radio. The AD7002* (Figure 3) +5-V single-supply I/O port has a/d and d/a converters and support circuitry designed expressly for the next generation of cellular phones, which will modulate the carrier with digitized and coded signals for transmission, in contrast to the analog information handled by today's phones. Interfacing between the encoding digital processor and the analog world of signal transmission, it is designed for systems that meet the pan-European GSM specification (see sidebar).

The AD7002, a complete two-channel input/output port with pulse shaping, is used as a baseband subsystem for signal conversion between the DSP and IF/RF subsections in the pan-European digital phone system. Since mobile phones must minimize power consumption, the *transmit*, *receive*, and *auxiliary* sections have separate power-down (sleep) controls.

*Use the reply card for technical data. Circle 1

Transmit Section This section consists of ROM, containing the code needed for performing Gaussian minimum-shift keying (GMSK), a form of frequency-shift keying that shapes pulses to minimize spectral leakage), plus two 10-bit d/a converters with output reconstruction filters.

The GMSK in-phase and quadrature (*I* and *Q*) waveforms, are generated at 16×oversampling, using differential encoding. The I and Q data streams drive the two d/a converters, with outputs filtered by Bessel low-pass linear-phase filters (300-kHz cutoff). The filters are essentially identical, tending to minimize the phase mismatch between I and Q channels.

Receive Path This path has two 12-bit a/d converters for the incoming I and Q signals, using sigma-delta architecture, and sampled at 13 MSPS. The converters are preceded by switched-capacitor filters and followed by digital filters, to provide the necessary input and system filtering. The converters for the *receive* and *transmit* paths share an on-chip bandgap reference.

Auxiliary Functions Three on-chip control d/a converters (8-, 9-, and 10-bit) are used in automatic frequency control (AFC), automatic gain control (AGC), and signal leveling. Besides handling signals, the AD7002's interface to the digital processor (serial, to minimize package pin count) includes a control channel to establish timing parameters, set auxiliary-DAC levels, and perform calibration. Hard-wired pins configure the *sleep-mode*.

AD7002 is housed in a 44-pin plastic quad flat pack (PQFP) and uses a single +5-V supply; it is priced at <\$20 in OEM quantities.

Thanks to Doug Grant and Bob Clarke of Analog Devices, Wilmington, MA, for valuable assistance and focus. The AD7002 was designed at Analog Devices B.V., Limerick, Ireland, by a team including Pat O'Connor, Raymond Speer, Hans Tucholski, Pat Weeks, and David Welland.

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2. Groshong, Richard and Stephen Ruscak, "Undersampling techniques simplify digital radio," *Electronic Design*, May 23, 1991, pp 67-78.
3. Kester, Walt (ed.), *Mixed-Signal Design Seminar*. Analog Devices, Inc., 1991, pp. X-11 through X-20. [For a copy, use the book purchase card]
4. *Analog Dialogue* 22-2, 1988, pp. 6-7. Use the reply card. Circle 2

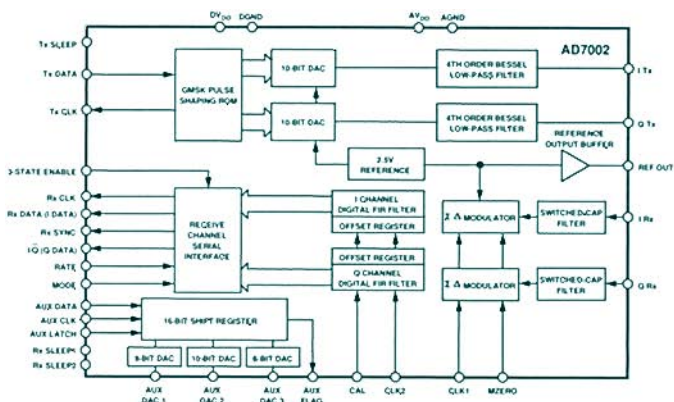


Figure 3. AD7002 input/output port.

Monolithic Sigma-Delta A/D Converters Offer 21-Bit Resolution

Sensor-to-serial devices feature conditioning for strain-gages, thermocouples, RTDs, and low-level signals

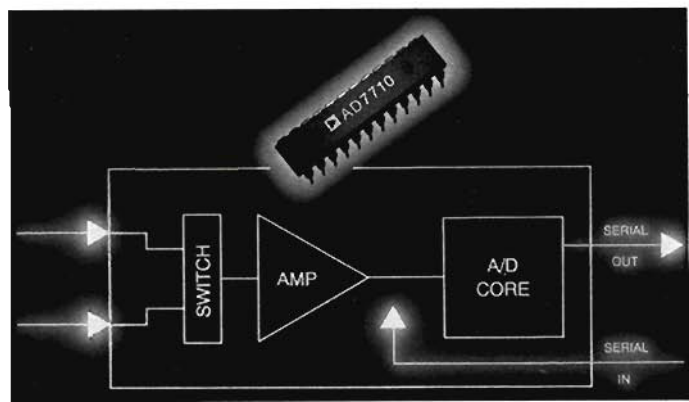
by John P. O'Connell

The AD771X family of monolithic sensor-to-serial ICs uses oversampling (sigma-delta) a/d converter technology to provide conversions with better than 21-bit effective resolution and no missing codes discernible to 24 bits. They are designed to interface the outputs of sensors such as load cells, RTDs, thermocouples, as well as other low-level signals, to a digital system directly via a bidirectional serial port. Each device type features an input structure with signal conditioning appropriate for a specific class of sensors. Available packages include 24-pin skinny DIP and 24-lead SOIC.

The family—which now comprises four device types, AD7710 through AD7713—provides a complete data-acquisition system solution. Besides a/d conversion, the ICs also include sensor signal conditioning and a programmable gain amplifier (PGA), plus a second input channel—useful for external signal calibration—as well as transducer failure detection. The devices are:

- AD7710: low-level data acquisition—e.g., strain gages and thermocouples
- AD7711: specifically configured for RTD temperature measurement
- AD7712: general-purpose data acquisition, large and small signals
- AD7713: general purpose, low-power, external reference

Each IC includes the digital filtering necessary to transform the high-rate stream of 1-bit conversions—inherent in the oversampling converter architecture [see sidebar]—into useful digitized



results. Filter cutoff and settling time can be adjusted by programming the first notch of the filter via an on-chip control register. To ensure that truncation and roundoff errors do not compromise converter performance, the digital filtering internally employs > 30-bit computation.

Each IC includes the a/d conversion core, calibration microcontroller with RAM, clock oscillator, digital filter, 2.5-V reference (except the AD7713), and a bidirectional serial communications port—which is used for setup, readback, and results. All-CMOS is employed for low power dissipation (3.5 mW for AD7713, 25 mW for the others), even lower with the power-down “sleep” mode (5 mW, 5 mW, 50 μ W, 35 μ W, respectively, for the AD7710, 11, 12, 13). The supply can be a single +5 to +10-V—or a dual \pm 5-V (except for the AD7713).

The Programmable Gain Amplifier: The PGA provides gains from 1 to 128 V/V in binary increments (set through the serial port), minimizing the need for external amplifier circuitry. The available input range is from 0 to +20 mV and 0 to +2.5 V in the unipolar mode, and \pm 20 mV to \pm 2.5 V for bipolar signals, with a 2.5-V reference applied. The AD7712 provides a high-level input channel for \pm 10-V signals, though operating from a \pm 5-V supply; and the AD7713 handles 0 to +10-V inputs with a +5-V supply.

The gain setting of the PGA impacts the effective resolution. For example, at a notch frequency of 50 Hz, the resolution increases from 15.5 bits (840 nV p-p in 20 mV) to 19 bits (7.5 μ V p-p in 2.5 V) as the gain decreases from 128 to 1.

Filtering: The user can set the cut-off frequency, location of the first notch, and the data rate of the programmable $(\sin x/x)^3$ digital

Table 1. AD7710 Effective Resolution vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate ¹	Effective Resolution ¹ (Bits)								
	-3 dB Frequency	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	21.5	21.5	21	20.5	19.5	18.5	17.5	16.5
25 Hz	6.55 Hz	20.5	20.5	20	20	19	18	17	16
30 Hz	7.86 Hz	20.5	20	20	19.5	18.5	18	17	16
50 Hz	13.1 Hz	19	19	19	18.5	18	17.5	16.5	15.5
60 Hz	15.72 Hz	18.5	18.5	18.5	18.5	18	17	16.5	15.5
100 Hz	26.2 Hz	16.5	16.5	16.5	16.5	16.5	16.5	15.5	15
250 Hz	65.5 Hz	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13
500 Hz	131 Hz	11	11	11	11	11	11	11	11
1 kHz	262 Hz	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5

NOTE

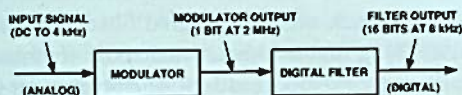
¹Effective resolution is defined as the magnitude of the output rms noise with respect to the input full scale (i.e., $2 \times V_{REF}/GAIN$). The above table applies for a V_{REF} of +2.5 V and resolution numbers are rounded to the nearest 0.5 LSB.

filter. These are controlled by a 12-bit word in the 24-bit control register. The first-notch frequency determines the output data rate; for example, if the notch is set at 50 Hz, a new output word—the digitized result—is provided every 20 ms. The first notch frequency can be varied from 9.76 Hz to 1.028 kHz, and the -3-dB cutoff frequency has a range from 2.56 to 269 Hz.

SIGMA-DELTA CONVERTER ARCHITECTURES

Traditionally, high-resolution (≥ 16 bit) a/d converters have been built using integrating and successive-approximation approaches. Common variants of the integrating approach have included dual- and quad-slope devices and voltage-to-frequency converters.

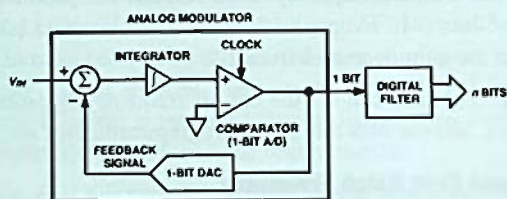
An architecture that has come into increasing use in the design and manufacture of converters is called *oversampling*, or *sigma-delta* (a.k.a. delta-sigma) in which a stream of bits, resulting from a large number of rapid one-bit conversions, is digitally filtered to produce a digital word of arbitrary length



Sigma-delta overview.

This approach to the problem of accurately transforming signals into their digital equivalents—with high resolution—involves a different technique. Instead of attempting to make unique measurements using high-precision components to obtain high resolutions, a converter employing this approach performs low-resolution (1-bit) conversions, but at a rate far greater than is required for the final higher-resolution word delivered digitally.

A simple example of such a one-bit converter is an analog modulator, similar to charge-balance circuits in V/f converters, but realized with relatively simple and low-cost circuitry. For example, the modulator might sample a dc-to-4 kHz signal and produce a stream of conversions at 2 MSPS; filtered digitally, this stream might result in an 8-kbps train of 16-bit words.



Sigma-delta modulator detail.

The modulator design is crucial to high performance, since it provides noise shaping, moving the bulk of the noise out of the baseband and into higher frequencies. They get filtered out by the digital low-pass filter, which transforms the hard-to-recognize rapid stream of one-bit conversion results into useful digital values corresponding to the analog signal. The filter also provides the flexibility to tailor the converter's spectral characteristics to the application (see the References below for much useful information).

Sigma-Delta Converter Features: Although this approach seems somewhat unwieldy, it offers some advantages over the conventional "precision" techniques. Some of these features can be found in conventional designs, but the sigma-delta architecture combines all of them:

Calibration: There are several available calibration options. The AD7710 can be directed to self-calibrate, using a basic two-point scheme: the input channel is shorted for a zero-point offset and the reference provides the full-scale setting. The second option, *system calibration*, eliminates external system offset and scale errors, using two points of the input range. Self-calibration can be

- the circuitry is predominantly digital (mostly in the digital filter), and the requirements on the 1-bit analog section are not tremendously rigorous. Thus converters can be built using processes customarily used for digital circuitry and even combined with purely digital functions, such as microprocessors, microcontrollers, and special-function digital peripheral circuitry (such as communications controllers).

- the digital filter can be designed to meet specific application needs, providing characteristics that are most useful for a specific kind of application. For example, if 50/60-Hz noise is a major problem, the filter design can be focussed on minimizing that noise, perhaps at the expense of other characteristics, such as settling time. The filter can also be user-programmable, and even adaptive, as changing filter coefficients can be written into internal registers. Once written, there is no drift or tolerance error (except for truncation and roundoff errors in recursive circuitry).

- these converters can be designed to produce a digital output that is inherently a monotonic function of the input, a requirement in many closed-loop control systems to prevent instability or even catastrophe.

- they are inherently self-sampling and tracking. There is no need for an external sample/hold or track/hold circuit. The high sampling speed results in low aperture errors.

- they are best suited for one-converter-per-channel use, which can improve system robustness, yet their cost is low.

- their serial output reduces the number of package pins needed for digital interfacing.

Of course, no single a/d converter architecture is ideal. Sigma-delta converters have some weaknesses:

- due to the history of bits that the digital filter needs, the latency period is relatively long between the first one-bit sample and the corresponding multibit digitized value. This makes it difficult to use the converter with a multichannel multiplexer, except where the second channel is used only rarely—since bits from the first channel must be "flushed" and bits from the new channel must flow into the filter pipeline.

- a given clock cycle cannot be immediately associated with a sample value, since the result lags the actual sampling period.

- at present, sigma-delta converters are limited in bandwidth and effective sampling rate (output word rate), compared to other architectures (especially when flash converters are included). Effective word rates equivalent to about 10 kbps are available now. Higher rates require extremely fast oversampling clocks and ICs for useful resolution.

- the resolution/accuracy/speed tradeoffs must be carefully judged by the system designer, since the device flexibility (primarily due to the digital filter) also implies a variety of performance envelopes.

done solely on start-up; it can also be set to run continually in a background mode, ensuring that the digitized readings are accurate even when the ambient temperature changes. In the latter mode, the time taken for calibration compels a tradeoff; the rate of new conversions is reduced by a factor of six.

Alternatively, the user can write zero- and full-scale calibration coefficients directly to the calibration registers, if system requirements show that an externally supplied calibration is more appropriate.

Specifications: Table 1 shows the effective resolution (in bits = $\log_2(\text{input full scale/output rms noise})$) achieved at various gains and notch-frequency settings for the AD7710. The converter family is specified to provide 24 bits of no-missing-code performance with $\pm 0.0015\%$ nonlinearity. Common-mode rejection (dc), for differential inputs, and normal-mode 50/60 Hz noise rejection, exceed 100 dB.

Output noise varies with gain and -3-dB cutoff frequency. At 2.62-Hz bandwidth and gains from 8 to 128, noise is $0.4 \mu\text{V rms}$; at unity gain it is $1.7 \mu\text{V rms}$; at 16 Hz and gains of 64 and 128, noise is $0.84 \mu\text{V}$, rising to $13.5 \mu\text{V}$ at $G = 1$.

AD7710* (Figure 1) provides two differential input channels and is designed for low-frequency measurement applications, such as a strain gage or thermocouple data acquisition (a $20\text{-}\mu\text{A}$ current is provided for use in cold-junction-compensation in the latter case).

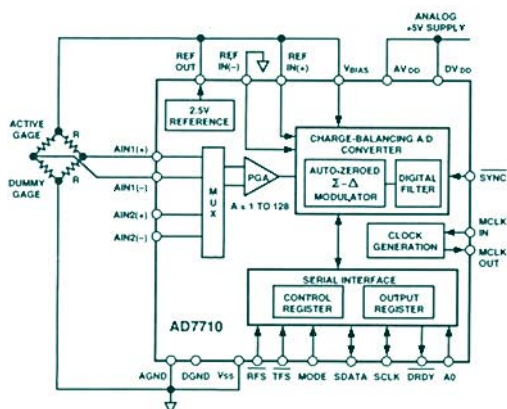


Figure 1. AD7710 block diagram, with strain gage connection.

One of the most useful features of the AD7710 (and its other family members) is the second input channel and multiplexer. This second channel is not intended primarily to form a two-channel converter for two input signals (although it can work in that mode). Rather, it is designed to let the user connect an external calibration signal to the converter input signal path, thus including the PGA in the calibration.

This is especially useful for transducer applications such as strain gages and load cells, for example—the primary transducer can be compared directly with a higher-accuracy lab standard or reference signal. Also, in many applications, the absolute magnitude of the signal may be of less importance than its value relative to a signal at the second channel.

AD7711† (Figure 2) is very similar to the AD7710. The main difference is that it is designed specifically for RTD (resistance-temperature-device) transducers. It provides a primary differen-

tial channel and a secondary single-ended channel, plus excitation current sources.

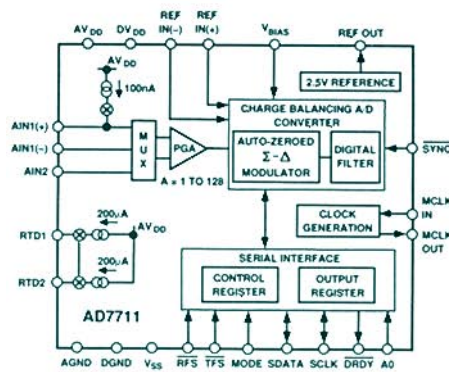


Figure 2. AD7711 block diagram.

The AD7711 can support both 3- and 4-wire RTDs; a 4-wire configuration is shown in Figure 3. With a nominal $100\text{-}\Omega$ RTD and $200\text{-}\mu\text{A}$ current source, the potential across the RTD is 20 mV , easily handled by the AD7711 at high gain settings. Resistor R_{ref} is used to generate the AD7711 reference voltage using the second current source within the AD7711. This ensures that the analog input voltage span remains ratiometric to the reference voltage, compensating for any errors in the analog input voltage due to current-source drift.

AD7712 and AD7713‡: The AD7712 is designed for general purpose data acquisition and conversion. Two input channels are available—a differential channel for low-level signals, and a single-ended channel which attenuates to $1/4$ so that signals up to $4\times$ the reference can be accepted. The AD7713 provides two differential inputs, one high-level voltage-input channel, and two $200\text{-}\mu\text{A}$ current sources for RTD applications. The AD7713, optimized for low-power and 4-to-20 mA applications, is referenced externally. A Standby pin on these two devices allows them to be put into the low-power mode via hardware, as well as software.

The AD7710, AD7711, AD7712, and AD7713 are priced at \$15, \$16, \$14, and \$17, respectively, in 1,000-piece quantity. ▶

The AD771X family was designed by Damien McCartney, Pat Hickey, and Stuart Patterson at Analog Devices' facility in Limerick, Ireland.

References:

Kester, W. (ed.), *Mixed-Signal Design Seminar*, 1991, published by Analog Devices. Use the book purchase card

Candy, James C. and Gabor C. Temes (eds.), *Oversampling Delta-Sigma Data Converters—Theory, Design, and Simulation*. New York: IEEE Press, 1992.

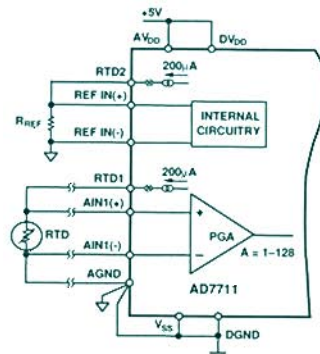


Figure 3. AD7711 with 4-wire RTD.

*For technical data, use the reply card. Circle 3

†For technical data, use the reply card. Circle 4

‡Use the reply card for technical data. Circle 5 for AD7712, 6 for AD7713

Applying a High-Performance Video Operational Amplifier

Using the AD811 as an ADC input buffer, dc restorer, and sync stripper

by Dave Whitney & Walt Jung

The recently introduced Analog Devices AD811*, using the most up-to-date circuit and process technology, is the highest performer in a growing line of monolithic transimpedance amplifiers. It is intended primarily for high-speed ac applications, like its predecessors—for example, the AD844, the AD846, the OP-160/OP-260, and the AD9617/AD9618.

While its principal uses are likely to be broadcast, studio and HDTV video signal processing, it should also find uses in many other applications that require wide bandwidth, low distortion, and the ability to handle large signals at high speed. Some examples of demanding applications include signal generators and other lab instruments, radar, IF, and ultrasound amplifiers, medical instrumentation, gamma detectors, ADC & DAC input/output buffers.

Built on Analog Devices' proprietary high-speed complementary bipolar (CB) process, the AD811 achieves new highs for overall performance. It combines a gain-bandwidth of over 100 MHz, a slew rate (SR) of 2500 V/ μ s, and an output-current capability of more than 100 mA, with very low distortion. In addition, the AD811 settles quickly and cleanly; for a 2-V step, settling time is 25 ns to 0.1%, and for a 10-V step it settles in just 65 ns to 0.01%.

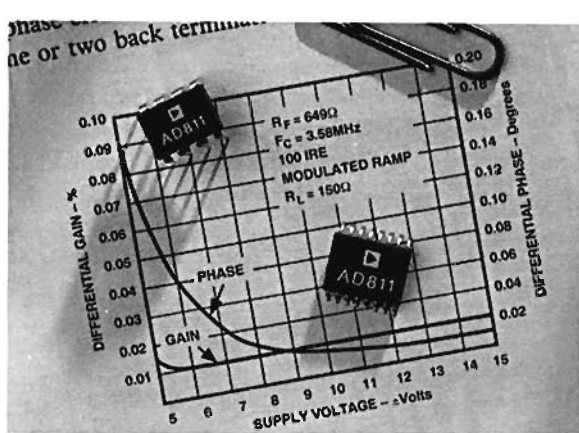
The AD811 is available in two temperature grades with similar electrical specs. The AD811A and AD811S are respectively specified for -40 to +85°C and -55 to +125°C. The variety of packages includes 8-pin plastic and cerdip, 16- and 20-pin SOIC, and 20-pin LCCs. Prices start at \$2.85 in 1000s.

Most important among the device's specifications are those illustrating its applicability for premium levels of performance in demanding video applications. The AD811's differential gain and

Table 1. AD811 amplifier recommended resistor values and resulting -3-dB bandwidth for various closed-loop gains and $V_S = \pm 5$ V and ± 15 V.

$V_S = \pm 15$ V	R_{FB}	R_G	- 3 dB BW (MHz)
Closed-Loop Gain	(ohms)	(ohms)	
+1	750		140
+2	649	649.	120
+10	511	56.2	100
-1	590	590.	115
-10	511	51.1	95
$V_S = \pm 5$ V	R_{FB}	R_G	-3 dB BW (MHz)
Closed-Loop Gain	(ohms)	(ohms)	
+1	619		80
+2	562	562.	80
+10	442	48.7	65
-1	562	562.	75
-10	442	44.2	65

*Use the reply card for technical data. Circle 7 for the AD811.



phase are rated at less than 0.01% and 0.01° respectively (closed-loop gain of 2 V/V at 3.58 MHz, $R_L = 150 \Omega$). In addition, its gain flatness is held within ± 0.1 dB to 35 MHz (typical)—a performance parameter important for HDTV systems. The above features are available to designers of many kinds of circuits and systems, since the AD811 is rated to operate from a wide range of supplies: ± 5 V to ± 15 V. Though there is some performance degradation with the lower supply voltages, the part is characterized in the video bandwidth range for various gains at these supply voltages (Table 1). As a result, the user knows just what the tradeoffs will be (more on this below).

DESIGN HIGHLIGHTS

Though the circuit of the AD811 is basically similar to those of many other transimpedance ICs, the performance distinctions setting it apart come from attention to design details. For example, device trimming at the input stage results in low offset voltage (0.5 mV) and bias current (2 μ A), low numbers for this type of amplifier. For large, fast non-inverting signals, an input stage slew-enhancement circuit comes into play, allowing closer signal tracking and lower distortion when it is used as a follower. This eliminates a common problem among transimpedance amps when they operate as followers.

Transimpedance amplifiers as a rule aren't noted for high gain accuracy, for either dc or ac. Open-loop gain in a transimpedance amplifier is maximum when the transresistance, R_t , is high (under load at the output), and the inverting node input resistance (R_{IN}) is low. In the AD811, the typical figures for these parameters are 1.5 M Ω and 14 Ω , respectively. As a point of reference, some commercially available transimpedance amplifiers only achieve transresistances of a few hundred kilohms when loaded (though they may boast high figures when unloaded). Although the AD846 sports a landmark R_t of 200 M Ω while driving a 500- Ω load, the AD811's albeit lower R_t is achieved driving 200 Ω ; and the AD811 has, in addition, the combination of outstanding specs noted above.

While high R_t implies high open-loop gain, hence high gain-accuracy, low R_{IN} values allow the amplifier to maintain more bandwidth as closed loop gain is raised—a salient trait of the transimpedance topology.

The AD811's output uses a parallel array of high-speed, large-geometry complementary transistors with current limiting set at ± 150 mA. The resulting high gain-linearity and low output impedance allow loads of 100 Ω to be driven to ± 10 -V levels with low distortion. The stage's low 9- Ω open-loop output resistance

contributes to load immunity. In addition to the NTSC differential gain and phase video specs already cited, the 10-MHz distortion of the AD811 is also low, at -74 dBc; and the third-order intercept is 43 dBm.

VIDEO PERFORMANCE

For video designers, a relevant aspect of the AD811 is that it is fully specified for typical "bread-and-butter" video uses, that is, the circuit environment needed for a direct performance assessment. Figure 1 illustrates this point, showing a standard application of a gain-of-2 video buffer or line driver. This circuit replicates a standard NTSC video signal, V_{IN} , with the input line terminated in $75\ \Omega$. The AD811 stage operates at a gain of 2, driving a pair of $75\text{-}\Omega$ output lines with $75\text{-}\Omega$ back terminations. V_{OUT1} and V_{OUT2} are thus individually isolated/buffered unity-gain versions of V_{IN} . With the overall terminated gain of unity, this circuit serves well as a low-distortion buffer, or a video-distribution amplifier.

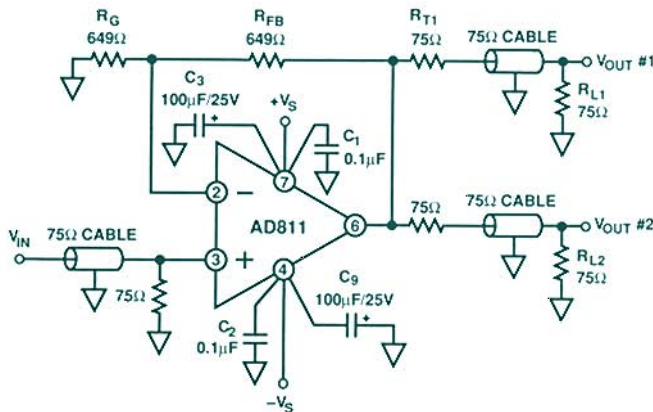


Figure 1. A video line driver operating at a gain of +2.

Connected as shown and operated from $\pm 15\text{-V}$ supplies, the circuit has a -3-dB bandwidth of 120 MHz, and differential gain/phase of $0.01\%/0.01^\circ$ with one line driven ($R_L = 150\ \Omega$). Driving two lines, the gain errors are essentially the same, while the phase errors rise to about 0.04° . The gain flatness (ripple-free) of this circuit is to within 0.1 dB at frequencies up to 35 MHz with $\pm 15\text{-V}$ supplies. As one might expect, lower supplies do degrade performance somewhat, but differential phase is still less than 0.18° with $\pm 5\text{-V}$ power. The -3-dB bandwidth falls to 80 MHz, and 0.1-dB gain flatness is maintained to 25 MHz. Nevertheless, essentially full video capability is achieved for supplies above $\pm 10\text{ V}$.

Table 1 summarizes bandwidth performance for this basic circuit for a variety of other gain options (up to $\pm 10\text{ V/V}$), for both power supply levels. The resistance values chosen for the various gains are standard values for 1% tolerance, for straightforward circuit assembly. For best accuracy and stability, metal-film resistor types are recommended.

Construction of this and other AD811 circuits should be in accordance with high-speed rules. A solid, heavy copper ground plane should be used, and circuit layout should be compact with low capacitance. In addition, the power supplies should be well bypassed. As a minimum, local low-inductance, low-ESR rf bypass caps (C_1 and C_2) should be used right at the device supply pins. These are $0.1\text{-}\mu\text{F}$ surface-mount chips (or other low-inductance

*Use the reply card for AD773 technical data. Circle 8

types). When driving high peak current loads, these high frequency bypasses should be augmented by local, short-lead/large-value low-ESR electrolytics such as C3/C4, in the range of $47\text{-}100\ \mu\text{F}$. These capacitors will carry the transient currents, and can be either tantalum- or aluminum types rated for high frequency (i.e., switching-supply types).

Power management can be important with the AD811, as it can dissipate fairly large power levels, even with relatively light loading. The quiescent current drain, relatively independent of voltage, is about 15 mA. Thus the power consumption is 150 mW at $\pm 5\text{ V}$, and slightly more than 3 times this at $\pm 15\text{ V}$. To minimize dissipation with minimal loss of performance, video applications with low output swings can use supplies of ± 10 to $\pm 12\text{ V}$, which yields the best performance for the least power. For applications requiring $\pm 15\text{-V}$ supplies, the lower-thermal-resistance cerdip and LCC packages should be considered. Alternatively, a small heat sink, such as the Aavid #5801, will be helpful when used on the plastic DIP package.

HIGH PERFORMANCE ADC INPUT BUFFERS

Nearly as demanding as (or perhaps even more demanding than) line drivers are analog-digital-converter (ADC) input buffers. Desirable maximum distortion levels are in the -60 to -70-dB range for 1-V-full-scale signals at up to 10 MHz or more. In addition, high speed ADCs are usually difficult to drive because of the dynamic load they often present, including current pulses or non-linear input capacitance; often they require differential-mode operation; and (quite important) they often use supplies of 5 V. All of these factors place demands upon the buffer amplifier used in driving the converter.

The circuit of Figure 2 is useful for driving high speed 10-bit ADCs. It was developed specifically as an interface to the differential-input AD773*, a 10-bit-resolution 18-MSPS ADC with pipelined-architecture (*Analog Dialogue* 25-2, p. 14). With minor variation, the circuit can be used with other converters, with both single-ended and differential-mode inputs. It can work directly from $\pm 5\text{-V}$ supplies, avoiding the destructive ADC over-drive possible with buffers requiring higher supply-voltages.

The AD773 operates best when driven differentially between inputs V_{INA} and V_{INB} , with full scale signals of $\pm 500\text{ mV}$. The paired-AD811 driver translates a $\pm 500\text{-mV}$ single-ended signal across R_{TIN} to dual $\pm 250\text{-mV}$ signals at V_{INA} and V_{INB} .

In high-performance differentially driven applications, the two output signals should maintain flat gain and linear phase—as well as low signal distortion—to above the highest frequency of interest. In this driver, the AD811s used for U1 and U2 operate as gain/phase-matched buffers with precise gains of ± 1 . While the inverter, U2, is conventional, the follower circuit, using U1, has a distinction that significantly impacts overall performance.

Normally a transimpedance amplifier, such as the AD811, connected as a unity-gain follower, would use just a single resistor for feedback (R_{FB1}). Here however, a dummy input resistor R_{G1} is added, providing improved gain/phase matching between the two amplifiers.

This gain/phase matching is quite effective, with results of 0.05 dB and 0.5° between the two output signals at 20 MHz, for a given pair of amplifiers, loaded as shown. These figures are 5-10 times better than they would be with the use of a conventional

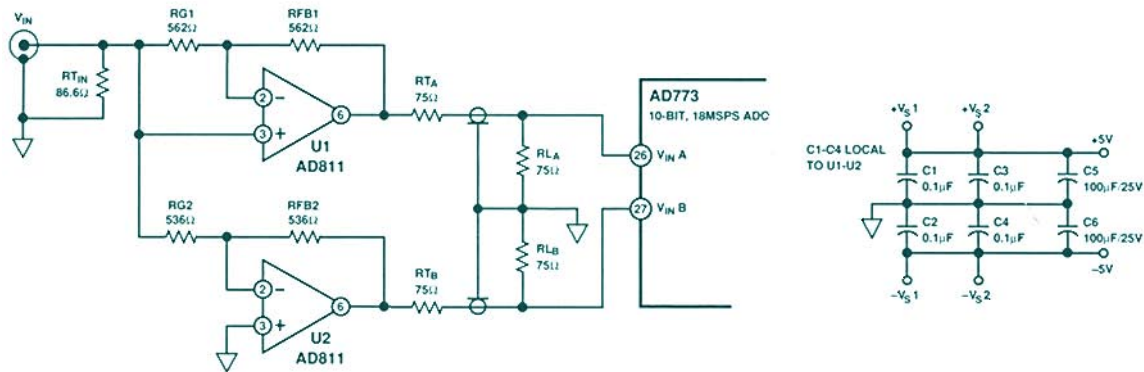


Figure 2. Optimized AD811 differential ADC buffer.

follower (i.e., sans RG1). Bandwidth of this driver is 80 MHz at the -3-dB point, and the 0.1-dB bandwidth is 25 MHz. Using this buffer with the AD773, second-harmonic distortion results at 8 MHz showed an improvement of about 15 dB over simpler drive schemes.

While this example shows an AD811 driving an AD773 directly, it is worth noting that, because of the line driving-capability of the AD811, the driver can be located remotely from the ADC if necessary.

SYNC TIP DC RESTORER

A common video signal-processing requirement is dc restoration, or clamping of ac-coupled signals. When used with a composite NTSC video signal, sync-tip clamping is commonly used. This fixes the most negative excursion of the signal—during the sync pulses—to a fixed dc level, usually ground. The rest of the signal, including the intensity-modulated picture information, is restored to the correct dc level. The circuit of Figure 3 is an example of a sync tip clumper, using 2 IC op-amps and two discrete transistors. With a standard NTSC composite video signal applied at J1, the circuit dc-restores the signal to a ground reference and makes the dc-restored and buffered version available at J2, source-terminated by 75 Ω.

In operation, the U1 stage functions as an ac-coupled input line isolator and buffer. The signal at J1 is attenuated to one-half by R1 and R2, and is ac coupled into U1, an AD811 configured as a wideband gain-of-2 amplifier [$G = 1 + R_4/R_3 = 2$]. With the values shown for R4/R3 and the use of ±10-V (or more) dc

supplies, the 1% bandwidth of stages U1 (and U2) will be more than 30 MHz.

The output of U1 drives Q1, a shunt JFET switch, through a film coupling capacitor, C2. The N-channel JFET is a low-capacitance, high-transconductance unit, chosen for on resistance of 50 Ω or less. The low capacitance allows it to be easily driven from U1, minimizing possible distortion of the signal. The low on-resistance of Q1 and high output current of the AD811 driver stage allows very fast charging of capacitor C2 between sync tips, at a rate that will be limited to $I_{max}(U1)/C_2$ V/s. With a ±100-mA output from the AD811 and a 0.1-μF value for C2, this allows maximum charging rates of the order of ±1 V/μs during the interval when switch Q1 is on (the clamp sample period). If this period is 0.1 μs, for example, the circuit can correct ±100 mV of baseline change for each clamp sample.

Since the overall video signal has a magnitude of the order of 1 volt p-p and varies rapidly relative to the correction rate, these design limits are conservative in practice. For example, suppose an interfering 60-Hz normal-mode hum adds a slowly varying 1-volt-peak sine wave to the rapidly-varying video waveform. The clamp circuit will seek to restore the waveform to ground during the sync interval at the end of each line; but during the following line, the output baseline will follow the 60-Hz signal increment. The clamp circuit will thus see a maximum rate of change, or slew rate of

$$SR = 2\pi f V_{peak}$$

For 60 Hz and 1 V, the rate of change is 377 V/s. In an NTSC 63.5-μs line interval, the maximum change of this hum signal is

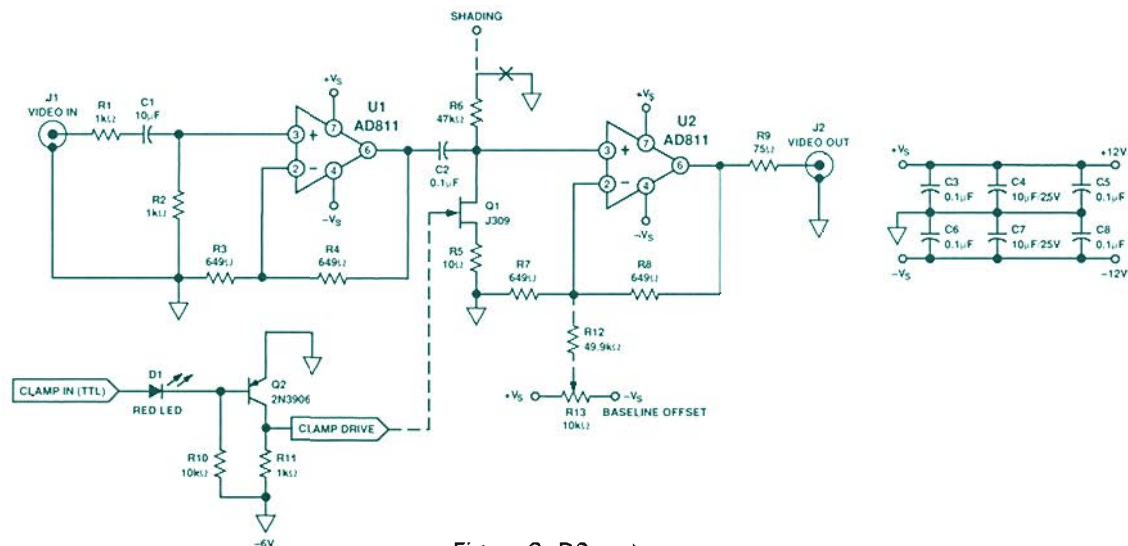


Figure 3. DC restorer.

$377 \times 63.5 \times 10^{-6} = 0.024 \text{ V}$, which is well within the range of correction.

The clamp's sample-period drive signal, derived elsewhere in the system, is presented to this circuit as a TTL signal at D1-Q2, *CLAMP IN*. It is an active-low TTL logic signal, timed to occur during the video waveform's negative sync tips. The low state signal drives both Q2 and Q1 on, effectively connecting C2 to ground through Q1-R5, and so provides the dc reference path to ground described above.

During the remaining interval of the horizontal sweep, the switch Q1 is off, due to the -6-V bias set via R11. The bias current of U2 is the main dc load on the C2-R6 voltage node during this time, tending to charge C2 positively or negatively with the bias current of U2. Since its magnitude could be as high as $5 \mu\text{A}$, the baseline ramp error ("droop") in $50 \mu\text{s}$ could be $[(I/C) \Delta T]$

$$(5 \times 10^{-6} \text{A} / 0.10 \times 10^{-6} \text{F}) \times 50 \times 10^{-6} \text{s} = 2.5 \times 10^{-3} \text{V},$$

or 2.5 mV . However, this is not likely to be a problem, as the typical AD811 bias current is lower, and the video signal is appreciably larger in amplitude.

On the other hand, if an intentional ramp-up or -down waveform is desired, to produce a horizontal shading (a black-to-white or white-to-black background), R6 can optionally be returned to a variable dc voltage to achieve this effect (by breaking the ground and applying the voltage at "X").

Another option possible with the circuit is to introduce a variable dc baseline to the clamped signal, for example to provide a specific bias point for a following stage. The optional bias network, consisting of resistors R12 and R13, can provide this function. The variable dc voltage from R13 injects a current through R12, adding to the output of U2, effectively allowing signal baseline offset of $\pm 150 \text{ mV}$ about the dc clamping potential (which otherwise is ground). If this feature is used, the value of R7 may require some adjustment for exact signal gain; also, the dc voltages, $\pm V_S$, should be clean.

The output stage, U2, is a second wideband AD811, configured as a $75\text{-}\Omega$ line driver in this case. U2 presents the DC restored video signal to the line at J2, with a level equal to the original signal at J1.

SYNC STRIPPER CIRCUIT

Another common video signal-processing requirement is the function of sync stripping. In a sync stripper, horizontal and vertical

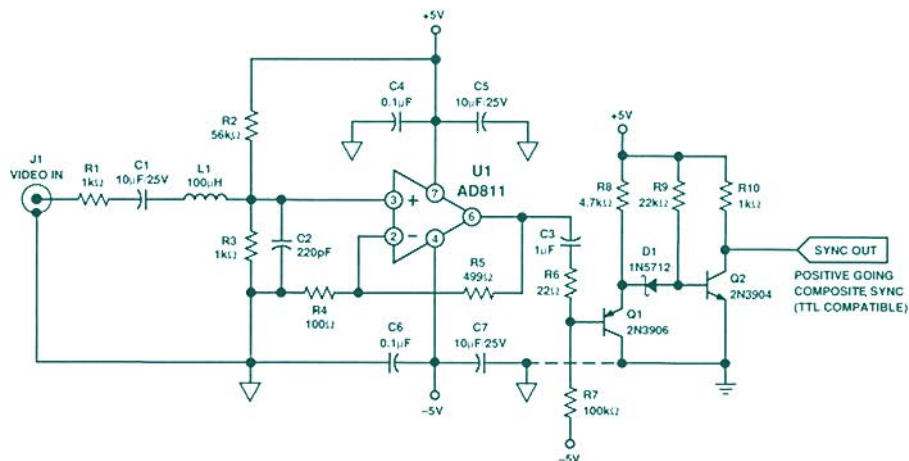
timing information is removed from the composite NTSC video signal and converted to logic levels for further processing. The circuit of Fig. 4 is a self-contained sync stripper, using one IC and a pair of discrete transistors. It is driven from an NTSC composite video signal at J1 and delivers TTL-compatible positive-going sync at the output.

In this circuit the U1 stage performs three functions. First, components L1-C2 act as a low-pass filter, reducing the 3.58-MHz chrominance components. U1, an AD811, is both an isolator with gain and a buffer to drive the following stage, which is a low-input-impedance sync tip clamp. The input signal at J1 is divided by a nominal factor of 2 by R1 and R2-R3, and ac-coupled to the input of U1. U1 is configured as a wideband $\times 6$ amplifier, by the R2-R4 ratio. This yields an overall luminance signal gain of $3\times$, from J1 to C3. With the gain values shown and $\pm 5\text{-V}$ (or more) dc supplies for U1, the stage can handle normal video signals without clipping at the output.

U1's output drives Q1, a PNP shunt clamp in an unusual configuration. In steady-state DC terms, Q1 is held in saturation by the bias current from R7, where the emitter is close to ground. Since the ac signal driving Q1 through C3 is a composite video signal with the sync tips the most negative limit, Q1 acts dynamically as a DC restorer. The negative-going video waveform sync tips drive Q1 into hard saturation, and when the more-positive parts of the waveform bring it out of saturation, it acts as a linear emitter follower. This action produces a dc-restored composite video signal at the emitter of Q1, with the sync tips referred to ground.

The output of Q1 is coupled to the base of NPN switch Q2, through Schottky diode, D1. The combination of this diode's forward drop and the V_{BE} of Q2 produce a switching threshold at the base of Q2 which, considering the signal levels, causes Q2 to switch on/off cleanly at about the sync tip's 50% amplitude point.

The output from Q2 consists of clean, noise-free sync timing information, positive-going during sync tips. This signal is TTL-compatible, by virtue of the $+5\text{-V}$ supply to Q2 as shown. Practical hints for getting the most from this circuit include paying attention to good decoupling of the U1 stage. The high instantaneous currents during the sync tips can generate power-supply and/or ground noise. Local bypassing of U1 with high capacitance to the logic-supply ground will help to control this, as will a compact layout and the use of a ground plane. ▶



An Analog Multiplier SPICE Macromodel

AD734 model permits multiplier functions to be simulated in system applications

by Adolfo A. Garcia

Besides operational-amplifier and voltage-reference macro models, the latest SPICE Model Library diskette from Analog Devices* includes a model of the AD734, a monolithic wideband, 4-quadrant analog multiplier. The model, developed at our PMI division, is the first available SPICE macromodel of a popular commercially available analog multiplier. The model offers significant benefits to system designers because they can easily incorporate the behavior of analog functions such as modulation/demodulation, frequency doubling, and high-speed rms-to-dc conversion in a computer simulation of their actual circuit environment. System responses can be quickly evaluated under real-world transient and steady-state small-signal conditions, with considerable saving of design time.

The topology of the macro model adheres very closely to the block diagram of the AD734 (Figure 1). Each subsection of the device, including the denominator control (DD) and an internal voltage reference (ER), was modeled using techniques developed to model op amps. To speed simulation time, we have used only passive elements and controlled sources—and as few active devices as possible—throughout the model. For example, the macromodel's input interfaces, X, Y, and Z, were designed to model the AD734's input offset voltages, input bias currents, common-mode rejection, and 40-MHz input bandwidth, using only resistors, capacitors, and controlled sources. Similarly, we based the design of the macromodel's output amplifier (the AD734's W interface) on the op-amp macromodel's gain and output stage topology to be able to predict accurately the AD734's output-voltage swing, open-loop voltage gain, short-circuit current, 10-MHz -3-dB bandwidth, and 450-V/ μ s slew rate.

active and passive components to derive the transfer function, $W = XY/U$, a transistor-level model for the translinear core wouldn't be practical; it would result in such slow simulation time as to make computer analysis of analog functions involving the normal feedbacks around the device (in a frequency-doubler application, for example) very CPU-intensive and time-consuming. The actual model of the multiplier core is shown in Figure 2; it was synthesized using only 8 components to derive the same transfer function and gain-bandwidth product.

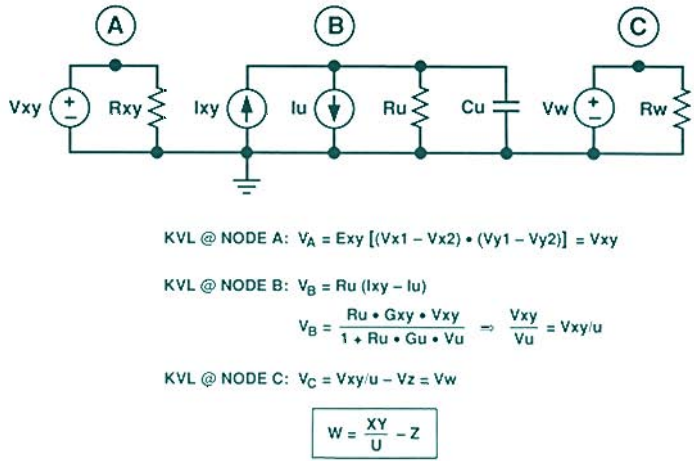


Figure 2. Modelling the AD734's multiplier core.

To explain how the multiplier core works, Kirchhoff's voltage-law (KVL) equations will be used. The voltage at node A is:

$$V_A = E_{XY} \times (V_{X1} - V_{X2}) \times (V_{Y1} - V_{Y2}) \equiv V_{XY}$$

where the coefficient, E_{XY} , has been set to 1.

To arrive at the KVL equation for node B, V_A is first converted to a current by transconductance, G_{XY} , viz., $I_{XY} = G_{XY} \times V_A$. A second controlled source, G_U (a second-order polynomial), is used to generate a current, $I_U = G_U \times (V_U \times V_B)$. The dc KVL equation at Node B is given by:

$$V_B = R_U \times (I_{XY} - I_U)$$

Substituting $G_{XY} \times V_A$ for I_{XY} , and $G_U \times (V_U \times V_B)$ for I_U , yields:

$$V_B = R_U \times (G_{XY} \times V_A - G_U \times V_U \times V_B)$$

Solving for V_B :

$$V_B = \frac{R_U \times G_{XY} \times V_{XY}}{1 + R_U \times G_U \times V_U}$$

Setting G_{XY} and G_U to 1 and R_U to 1E12 simplifies the expression for the voltage at node B to:

$$V_B \equiv \frac{V_{XY}}{V_U} \equiv V_{XY/U}$$

In the AD734, the high-gain output op amp nulls the difference between $X Y/U$ and an additional input, $Z = Z_1 - Z_2$, to generate the final output, W . This is done in the macromodel by subtracting the Z -input signal from XY/U , using another controlled source, E_W . Hence, the voltage at node C is given by:

$$V_C = E_W \times (V_{XY/U} - V_Z)$$

and, as was done for E_{XY} , the coefficient, E_W is set to 1. To complete the multiplier core, a capacitor, C_U , was added across

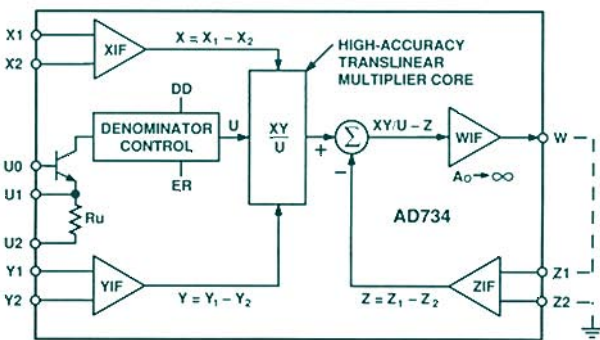


Figure 1. Block diagram of the AD734.

The translinear multiplier core at the heart of the AD734, based on the Gilbert multiplier cell, exhibits a 250-MHz gain-bandwidth product. Because the AD734's core employs approximately 50

*Use the reply card for the diskette and the AD734 data sheet. Circle 9

R_U to model the 250-MHz gain-bandwidth product of the AD734.

Figure 3 shows the connections configuring the AD734 as a three-variable analog multiplier/divider by using direct denominator control, with an additional offset-nulling feedback to X2 via A1 to permit evaluation of the macromodel's small-signal response. Compared to actual measured data of a typical device for four denominator settings, the model shows excellent agreement (Figure 4).

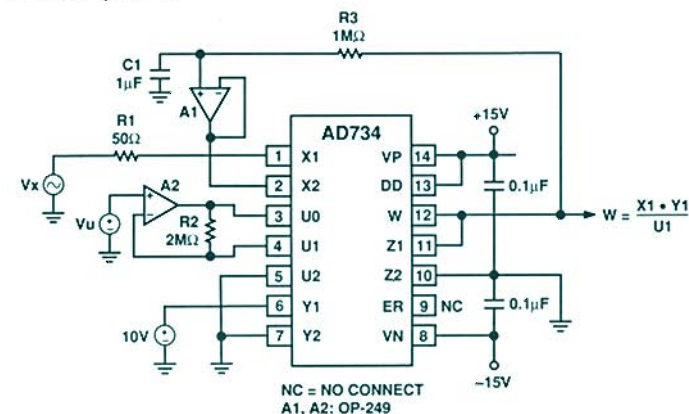


Figure 3. Circuit schematic of the AD734 configured as a three-variable multiplier/divider by using direct denominator control.

Among the many applications of analog multipliers, frequency-doubling of sinusoidal signals is quite often required in communication systems. The AD734 is ideal for this application and is typically configured as a squarer with the X and Y inputs wired in parallel. For sine waves, the ac component of the output signal of the AD734 is then a sine wave at twice the input signal frequency. In the circuit of Figure 5, for a 100-kHz, 20-V_{p-p} sine-wave, input phase shifting eliminates the output dc level associated with multiplying in-phase signals; and the R3-R4 attenuator rescales the output amplitude to equal the input.

As Figure 6 shows, the macromodel accurately simulates the AD734's behavior as a frequency doubler. The frequency-shaping stages in the macromodel permit custom tailoring of the AD734's small-signal and transient response with a high degree of accuracy.

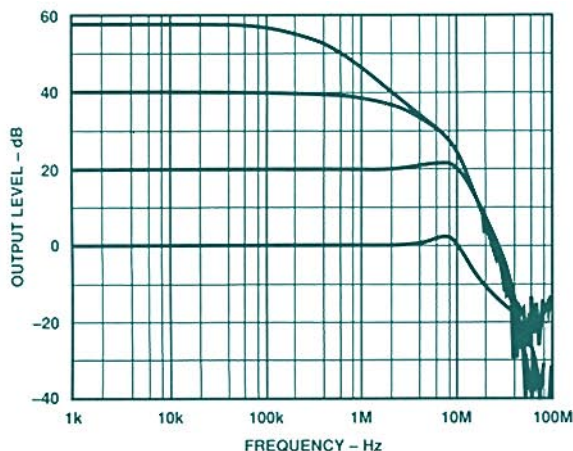


Figure 4. Three-variable multiplier/divider performance of the AD734 (Left, actual response; right, simulated model response).

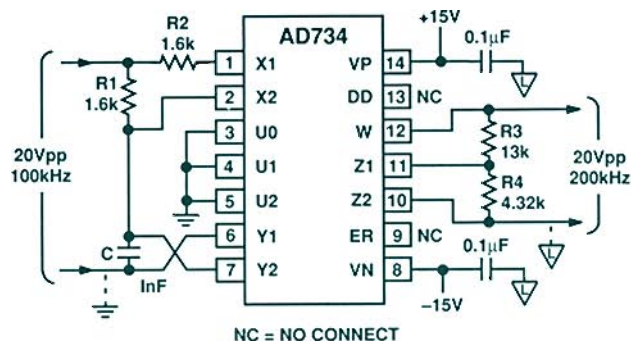


Figure 5. Circuit diagram of the AD734 configured as a frequency doubler.

The macromodel, in accurately modeling the AD734's small-signal and transient response, as well as incorporating its dc parameters, is a very powerful tool for evaluating and analyzing complex analog circuits and systems. Accurate prediction of real circuit behavior under small-signal and transient conditions provides a high level of confidence in a design for analog system or design engineers and can greatly speed up the breadboarding phase. We look forward to a continually expanding repertoire of macromodels for new linear and nonlinear analog ICs.

All simulation output charts were generated by MicroSim Corporation's PSpice circuit simulator.

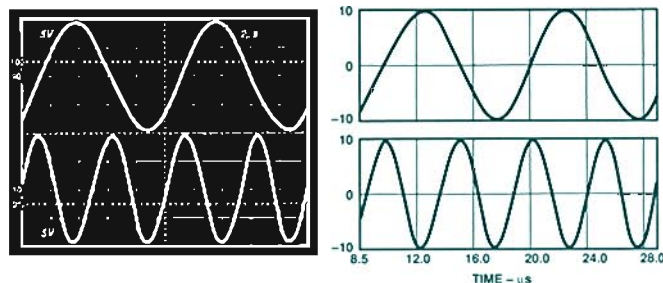
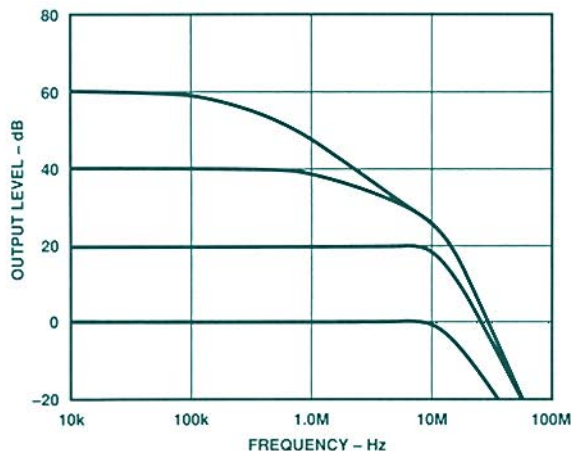
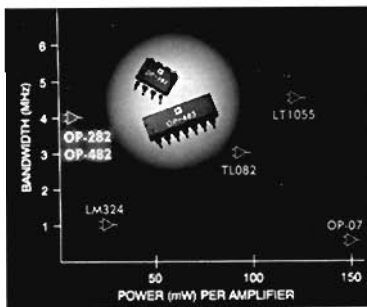


Figure 6. Waveforms at left show the AD734's frequency-doubler response to a 20 V_{p-p} input sine wave at 100 kHz. Macromodel (right) shows excellent agreement.



4-MHz Op Amps Low-dissipation JFETs OP-282/482 dual/quad



The OP-282 and OP-482* are dual- and quad FET-input operational amplifiers. Drawing only 250 μA maximum per channel, they are industry's lowest-dissipation 4-MHz unity-gain bandwidth op amps—with slew rate of 9 V/ μs and settling time of 1.6 μs to 0.01%. They are also low in cost. OP-482 prices in 100s start at \$1.95 (\$0.49/channel).

With their high input impedance and low bias current (500 pA maximum, -40°C to $+85^\circ\text{C}$, typically only 3 pA at $+25^\circ\text{C}$), typical applications include active filters, integrators, and buffer amplifiers.

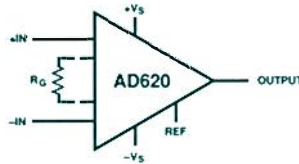
The devices will operate over a supply range of $\pm 4.5\text{ V}$ to $\pm 18\text{ V}$, with output swings to within 1.5 volts of the supplies. With their low power consumption, the amplifiers are well-suited for power-restricted and battery-operated applications. The upper end of the input common-mode range includes the positive supply; this makes the amplifiers an excellent choice for supply-current monitoring and high-side signal conditioning.

Maximum offset voltage is 3 mV for the OP-282 and 4 mV for the OP-482, with 4.5 and 6 mV max over temperature. Full-power frequency (1% distortion) is 125 kHz; and the amplifiers are internally compensated, with 55° phase margin. Noise is 1.3 μV p-p, 0.1 to 10 Hz, with a spectral density of 36 nV/ $\sqrt{\text{Hz}}$ at 1 kHz. Noise current is a low 10 fA/ $\sqrt{\text{Hz}}$.

Both devices are available for the -40 to $+85^\circ$ and -55 to $+125^\circ$ temperature ranges. The dual OP-282 is available in an 8-pin plastic DIP, cerdip, or SOIC; the quad OP-482 is available in a 14-pin DIP, cerdip, SOIC, or 20-contact LCC.

*Use the reply card for data. Circle 10

Amps for Instrumentation in SO-8 AD620 In-Amp features high accuracy, low cost AD626 Diff-Amp for single supply, gains of 10, 100



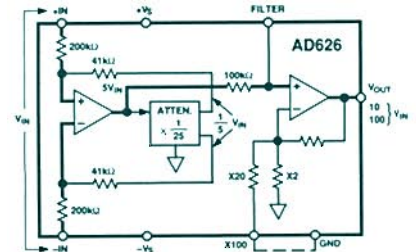
For applications where a difference between two voltages must be amplified in the presence of substantial common-mode voltage, one of these amplifiers will provide the lowest-cost solution—especially when compared with the expense to design and implement your own circuit. Both are available in 8-pin plastic mini-DIPs and SOICs for -40 to $+85^\circ\text{C}$; and the AD620 is available in cerdip (883B) for -55 to $+125^\circ\text{C}$.

The AD620† high-accuracy Instrumentation Amplifier provides gains from 1-1000, set by one external resistor. Noise is low (0.28 μV p-p, 0.1 to 10 Hz and 9 nV/ $\sqrt{\text{Hz}}$ @ 1 kHz); bandwidth is 120 kHz ($G = 100$). With its max: 50- μV V_{os} , 0.6 $\mu\text{V}/^\circ\text{C}$ drift, and 1-nA I_b (B grade), and 40-ppm nonlinearity—and min 93-dB CMR ($G=10$, A grade)—it is ideal for such precision applications as weigh scales, transducer interfaces, ECG. The supply range is a wide

$\pm 2.3\text{ V}$ to $\pm 18\text{ V}$, at 1.3 mA max. Prices (1,000s) start at \$3.27.

The AD626‡ is a single-supply, low-power differential amplifier with on-chip gains of 10- and 100 V/V (externally modifiable). Supply range is $+2.4$ to $+10\text{ V}$ single, ± 1.2 to $\pm 6\text{ V}$ dual, drawing only 290 μA max). Uses include current sensing and sensor interfacing, especially in battery and portable applications. The common-mode range, 6 ($V_S - 1\text{ V}$), greatly exceeds the supply; for $+5\text{-V}$ supply, CMR = 24 V and output range is $+30\text{ mV}$ to $+4.7\text{ V}$ min. The inputs are overload protected (50 V continuous), and the internal attenuation network includes RFI filters. An external capacitor provides LP filtering. Prices (1,000) start at \$2.85.

†‡Use the reply card. Circle 11 for †, 12 for ‡

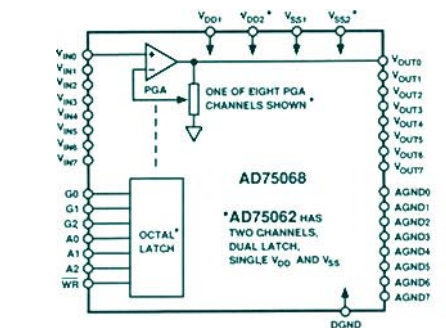


Multiple Programmable-Gain Amps AD75062/68: 2/8 channels of independent gain Gain range is binary, 1 to 128; constant bandwidth

The AD75062 and AD75068‡ are monolithic integrated circuits comprising 2- and 8-channels of independent digitally programmable gain amplifiers. The gains are set in 8 binary steps (viz., 1, 2, 4, . . . 128). Sonar and instrumentation are among the many applications.

The devices differ only in number of channels and package size. Each PGA channel is complete, including amplifier, gain-setting network, and control latch—and requires no external components. Small-signal bandwidth (-3 dB) is 2 MHz minimum at all gain values, with phase shift less than 2.5° to 10 kHz, 0.25° to 1 kHz.

MOS input bias current is less than 100 pA, -40 to $+85^\circ$. Nonlinearity is less than 0.04% at all gain values, and THD is



$< -75\text{ dB}$ at $G = 128$. Channel-to-channel isolation is 88 dB min, dc to 1 kHz. The AD75062 and AD75068 are housed in a 16-pin ceramic DIP and a 44-pin JLCC. Prices (100s) are \$20 and \$80, respectively.

‡Use the reply card. Circle 13

Two Fast 12-Bit Sampling ADCs

AD1671: Complete 1.25-MSPS lowest-cost IC

AD9034: 20-MSPS high-performance hybrid

These subranging flash ADCs greatly reduce the cost of 1-MSPS conversion and extend 12-bit conversion to the 20-MSPS range. They are complete with voltage references and sample/holds. Evaluation boards (with design details) are available for both.

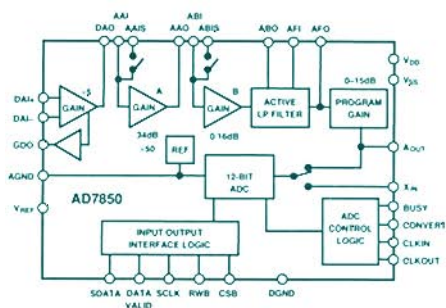
The **AD1671***, the lowest-cost converter in its class, offers 12-bit conversion at 1.25 MSPS with 70-dB minimum $S/(N+D)$ for a 100-kHz signal sampled at 1 MHz (K grade; J/A/S (all popular temperature ranges), offer 68 dB min). Housed in 28-pin cerdip, the AD1671 will also be available in PLCC. Prices (100s) start at a low \$55.

Features include low power consumption, (typically 570 mW); flexible input range (± 5 V, 0 to +5 V, high-impedance ± 2.5 V, 0 to +2.5 V); on-chip wideband sample-hold for undersampling applications (2 MHz full power and 12 MHz small signal); 2.5-V reference, which can also provide system reference; and an out-of-range flag.

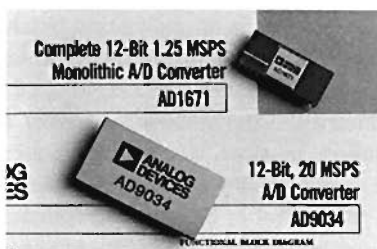
Complete 12-Bit Data Acquisition

AD7850: monolithic small-signal w/PGA, filter

AD1341: 16-channel, 150-ksps w/PGA, FIFOs

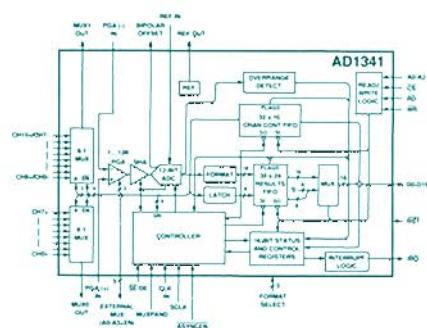


The monolithic single-channel **AD7850** is a complete data-acquisition system on a single CMOS chip. It includes a low-bias-current (1 nA over temperature) instrumentation amplifier with guard driver, filters (which can be configured for anti-aliasing), a programmable-gain stage, sampling ADC (66 kps min) with on-chip reference, and a high-speed microprocessor-compatible serial interface. Housed in a 28-terminal PLCC, it draws only 175 mW from the ± 5 -V supplies. Price (100s) is \$27.50.



The **AD9034†** is the highest-performance 12-bit, 20-MSPS a/d converter available at this writing, guaranteed and tested at a 20.48-MSPS conversion rate. Specs at 1 MHz include 65-dB minimum SNR, 80-dB SFDR, 74-dB min (B&T grades). For 10-MHz signals, they hold up well: 63 dB min, 76 dB, and 70 dB min. Power is low (4.5 W) from +5 and -5.2-V supplies. Packages are 40-pin ceramic DIP and leaded flatpack; industrial- and mil-temp ranges are available. Prices start at \$715 in 100s.

*†Use the reply card. Circle 14 for *, 15 for †

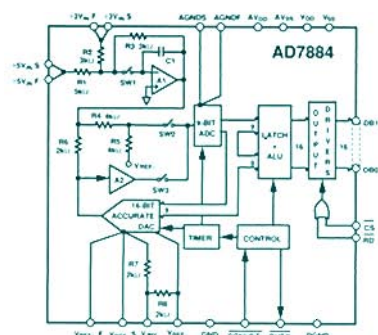


The **AD1341†**, a complete DAS, accepts 16 channels (8 differential) of input data, expandable to 32 (16) and converts with a throughput rate of 150 kps. It includes two 8-channel input multiplexers, a programmable-gain amplifier with binary gains up to 128 V/V per channel, SHA, data converter with reference and overrange detector, two 32-word FIFOs, a controller, and registers for status and control. It is housed in a 100-lead ceramic quad flat package. Prices start at \$198 (100s).

16-Bit SADCs

AD7884/5: 166 kps

Choice of 16/8-bit bus



The **AD7884/AD7885** are general-purpose 16-bit monolithic a/d converters with internal sample-hold, a conversion time of 5.3 μ s, throughput rate of 166 kps, and power dissipation of only 325 mW max (typically 250). The **AD7884** has a 16-bit parallel interface, while the **AD7885**—in a smaller package—is designed for 8-bit byte communication.

The **AD7884/7885** is fully specified for both static and dynamic performance, including such specifications as no-missing-codes over temperature (16 bits, -40 to +85°C), 84-dB min signal-to-noise ratio (SNR) -88-dB max total harmonic distortion (THD), -88 dB max peak spurious. The "B" grade has integral nonlinearity of 0.006% FSR max.

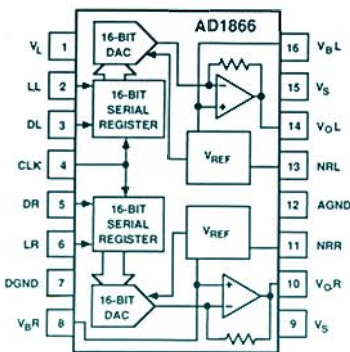
The **AD7885/7885's** speed and resolution make it useful in a great many high-resolution data-acquisition applications. Fast complete conversions make it suitable also for use with multiplexed analog inputs. Typical application areas include test equipment, DSP, medical instrumentation, industrial control, data acquisition, and robotics.

The **AD7884's** data-access time is 57 ns; it can interface directly to DSPs without servicing delays—saving valuable time for executing algorithms.

Accepting a reference of +3 V, the **AD7884/7885** can be pin-programmed to handle signals having ± 3 -V and ± 5 -V full-scale. Inputs and references have force-sense terminals to minimize lead drops. The **AD7884** is housed in a choice of 40-pin plastic DIP or 44-lead PLCC; the **AD7885** is available in 28-pin plastic DIP or PLCC. Prices (100s) for both start at \$45.

‡†Circle 16 for \$, 17 for ‡, 18 for †

16-b Stereo DAC AD1866: Dual, serial-in Complete, +5-V supply



The AD1866*, newest member of the Analog Devices SoundPort™ family, is a complete, high-performance, 16-bit dual stereo DAC, operating from a single +5-volt supply; it is designed specifically for portable, low-power, and computer audio (“multimedia”) applications. Since it requires no external components, it reduces audio system complexity and cost—a vital factor in portable-equipment applications. In addition, its low 50-mW power requirement produces further savings.

Complete on a single monolithic ABCMOS chip, the AD1866 contains CMOS logic elements, bipolar and MOS linear elements, and laser-trimmed, thin-film resistance elements. Careful design and layout techniques have resulted in low distortion and noise (0.005% THD+N, 95-dB SNR), high channel separation (115 dB), and low power dissipation.

Each DAC is equipped with a fast-settling, high-slew-rate output amplifier and requires no deglitcher. The buffered ± 1 -V output signal range is 1.5 to 3.5 V; and the on-chip 2.5-V references, available externally, make “false-ground” networks unnecessary.

A versatile serial digital interface (TTL- and 5-V CMOS-compatible) allows the AD1866 to be connected directly to all digital filter chips. Fast CMOS logic elements permit an input clock rate of up to 16 MHz, allowing for operation of each channel with 2, 4, 8, and 16 \times oversampling ($F_s = 44.1$ kHz).

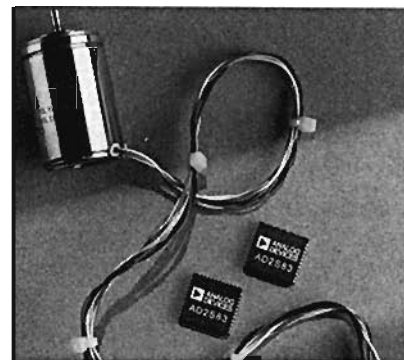
The AD1866 is housed in 16-pin plastic DIP or SOIC and is guaranteed to operate from -35 to $+85^\circ\text{C}$. Price (1,000s) is \$8.95. \blacksquare

*Use the reply card for technical data. Circle 19

Resolver/Digital Converter IC AD2S83 has high-performance velocity output User sets 10-, 12-, 14-, or 16-bit conversion

The AD2S83† is a monolithic tracking resolver-to-digital converter with a high-accuracy analog velocity output ($\pm 0.1\%$ nonlinearity, $\pm 0.3\%$ reversion error) and resolutions up to 16 bits, set by the user to meet system needs. Its principal application is in the control of brushless servo motors; velocity feedback maintains fast response and stability in the servo control loop—and the AD2S83 eliminates the size, cost, and maintenance of mechanical tachogenerators.

The AD2S83 converts resolver-format input signals (sine and cosine) to a natural binary digital word, using ratiometric tracking conversion [see *Analog Dialogue* 21-2 (1987), p. 25]. This ensures high noise immunity and tolerance of long leads, allowing the converter to be located at a distance from the resolver. The position output is available via 3-state switches, which can be configured for an 8- or a 16-bit bus.



The user can set the resolution at 10, 12, 14, or 16 bits, by the states of two control pins. By selecting external resistance and capacitance values, the user can determine bandwidth, maximum tracking rate, and velocity scaling. The AD2S83AP, specified for -40 to $+85^\circ\text{C}$, is housed in a 44-pin PLCC. Price is \$60.75 (1000s). \blacksquare

†Use the reply card for technical data. Circle 20

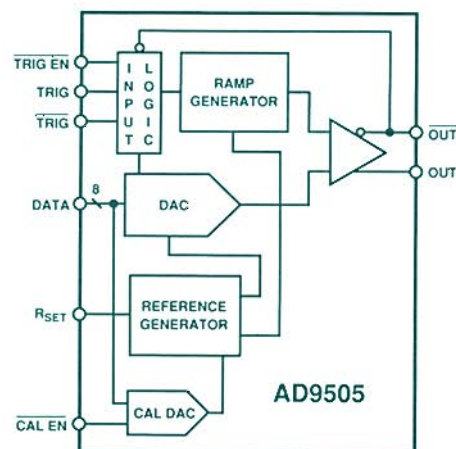
Digitally Programmable Delay IC AD9505 timing vernier can update “on-the-fly” Delay set by 8-bit data, 2.5- to 25-ns full-scale

The monolithic AD9505§ provides a digitally programmable delay between an input triggering edge and an output edge. The delay is proportional to the output of an internal 8-bit DAC, with a full-scale range of 2.5 to 25 ns—with 10-ps resolution of pulse-edge placement at 2.5-ns full-scale.

The time-delay value can be updated “on the fly”—with rated dynamic linearity—at each cycle of a 60-MHz clock rate (it can be clocked at up to 100 MHz, but with reduced linearity). The AD9505, using ramp-comparator-DAC architecture, is the newest member of the AD9500 family, introduced here in 1988 (vol. 22-1, pp. 14-15).

Range-programmable by a single external resistor, the AD9505 is complete—including an 8-bit DAC, internal reference, ramp generator with timing capacitor, a calibration DAC, and logic. It operates on a single -5.2 -V supply at 650 mW (780 max).

Applications include ATE (pseudo-random



pulse generation), printers and copiers (pulse manipulation in dot clock period for smooth gray-scale toning), disk drives (maximize storage with constant data density). A pair of AD9505s form a flexible programmable pulse generator. AD9505KP in PLCC for 0 to 70°C . 100s price: \$18. \blacksquare

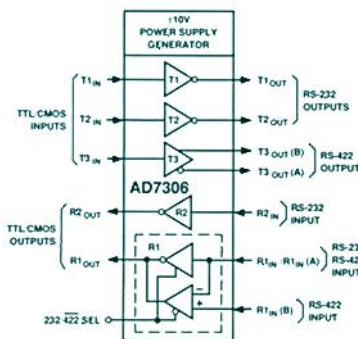
§Use the reply card for technical data. Circle 21

RS-232, -422 Line Driver/Receiver + 5-V-powered AD7306 includes charge pump ESD-, short-circuit-, and latchup-protected

The AD7306* is a monolithic multi-protocol RS-232/RS-422 driver-receiver chip, operating wholly from +5-volt power. Interfacing between TTL/CMOS signal levels and dual standard EIA RS-232/RS-422 signal levels, it is the first such chip to include a charge-pump supply to generate ± 10 V needed to develop RS-232 output levels.

The chip contains two RS-232 drivers and a receiver, an RS-422 driver, and a receiver path which can be configured to accept either. The RS-232 channels are suitable for rates up to 100 kHz, and the low-output-skew RS-422 channels are suitable for high-speed communications at up to 5 MHz.

The AD7306 is useful in applications where RS-232 and RS-422 signals are required in a single serial port—for example, bar-coders, printers, instrumentation—and especially with +5-V-only supplies. Users include manufacturers of computers and peripher-



als, remote sensors, and bar-code readers. Unlike many such supplies, the charge pump uses small 0.1- μ F capacitors, not needing space-devouring 10- μ F polarized types. Inputs are ESD-protected; outputs have high source- and sink capability and are short-circuit protected. The AD7306JR is housed in SOIC for 0 to +70°C. Price is \$4.25 in 100s. ▶

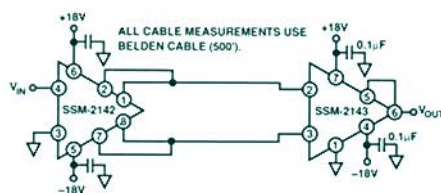
*Use the reply card for technical data. Circle 22

Differential Line Receiver Self-contained SSM-2143 works with SSM-2142 90-dB CMR (60 Hz), 6.5-MHz BW, 10-V/ μ s SR

The SSM-2143† is a high-common-mode-rejection differential amplifier with a gain of -6 dB (1/2 V/V)—a companion product to the gain-of-2 balanced-output SSM-2142‡ cable driver, introduced in *Analog Dialogue* 25-1 (1991), pp. 7 and 23. Together, the two devices provide a high-performance, low-cost, compact, overall unity-gain solution to preserving signal integrity over long cable runs in high-electromagnetic-interference (EMI) environments.

Though originally designed for analog signal transmission in professional, consumer, and automotive audio equipment, the SSM-2142/2143 system is equally applicable to other kinds of equipment employing voltage transmission with the potential of noise pickup over cable runs.

The SSM-2143's key characteristics include high common-mode rejection (90 dB typical, dc to 60 Hz, 85 dB at 20 kHz), ultralow distortion (0.0006% at 1 kHz), fast slew rate (10 V/ μ s), and wide bandwidth

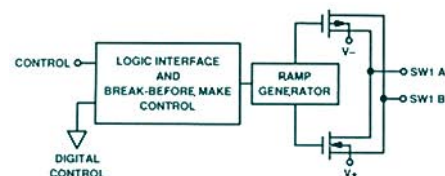


(7 MHz at $G = 1/2$). Although intended primarily for gain-of-1/2 applications, it can be connected for gain of 2 V/V by reversing the feedback connections.

Including thin-film resistors and precision laser trimming to maximize signal balance and circuit stability, the monolithic SSM-2143 replaces "roll-your-own" solutions requiring an op amp and four 0.005%-matched resistors. Specified for the -40 to +85°C extended industrial temperature range, the SSM-2143 is housed in an 8-pin mini-DIP—SOIC packaging soon available. Prices start at \$1.75 in 100s (PDIP). ▶

†‡Use the reply card for technical data. Circle 23 for †, 24 for ‡;

Audio Switch 4 Independent SPSTs SSM-2404 is "clickless"



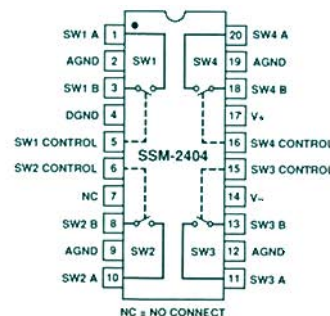
The SSM-2404‡ provides four independent SPST analog switches in a 20-pin plastic DIP or SOIC package. Unlike other analog switches, the SSM-2404 uses a ramp generator to produce a controlled switching transition to minimize transients caused by abrupt switching. For transparent audio switching—eliminating annoying audible clicks—the SSM-2404 (and its progenitor, the dual SSM-2402) are preferred to relays or conventional CMOS switches.

Not requiring external components for many applications, the SSM-2404 is easy to use—simply place one of its switches in the audio path and apply a TTL- or CMOS-compatible input to the appropriate control pin. Break-before-make operation is guaranteed.

Useful characteristics of the SSM-2404 include: ultralow THD+N [0.0008% (-102 dB) at 1 kHz, for 2 V rms, with 100-k Ω load], low charge injection (35 pC typically), high OFF isolation and low crosstalk (-100 dB and -94 dB at 1 kHz, $R_L = 10$ k Ω), low ON resistance (28 Ω typical), and low supply current (typically 900 μ A).

The device will operate on single or dual supplies (+11 to +24 V, or ± 5.5 V to ± 12 V). With an operating temperature range of -40 to +85°C, it is housed in a 20-pin plastic mini-DIP (SOIC available soon). It is conveniently priced at \$3.45 in 100s. ▶

‡Use the reply card for technical data. Circle 25



Ask The Applications Engineer—11

by James Bryant

All analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) require a reference signal, usually a voltage. The digital output of the ADC represents the ratio of the input to the reference, the digital input to a DAC defines the ratio of its analog output to its reference. Some converters have their references built-in, some require an external reference, but all must have a voltage (or current) reference of some sort.

Most early applications of data converters were in "dc" measurements of slowly varying signals, where the exact timing of the measurement was unimportant. Today most data-converter applications are in *sampled data systems*, where large numbers of equally spaced analog samples must be processed and spectral information is as important as amplitude information. Here the quality of the frequency or time reference (the "sampling clock" or "reconstruction clock") is comparable in importance to that of the voltage reference.

VOLTAGE REFERENCES

Q. How good must a voltage reference be?

A. It depends on the system. Where absolute measurements are required, accuracy is limited by the accuracy with which the reference value is known. In many systems, however, stability or repeatability are more important than absolute accuracy; and in some sampled-data systems the long-term accuracy of the voltage reference is scarcely important at all—but errors can be introduced by deriving reference from a noisy system supply.

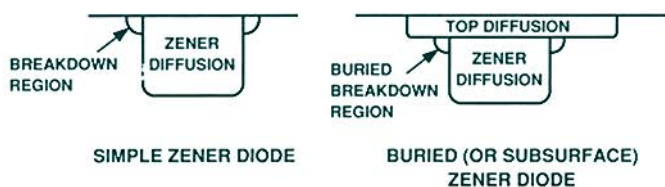
Monolithic buried-Zener references (for example the AD588 and AD688) can have initial accuracy of 1 mV in 10 V (0.01% or 100 ppm) and a temperature coefficient of 1.5 ppm/°C. They are accurate enough to use untrimmed in 12-bit systems (1 LSB = 244 ppm) but not in 14- or 16-bit systems. With the initial error trimmed to zero, they can be used in 14- and 16-bit systems over a limited temperature range. (1 LSB = 61 ppm, a 40°C temperature change in an AD588 or AD688).

For higher absolute accuracy, the temperature of the reference may need to be stabilized in a thermostatically controlled oven and calibrated against a standard. In many systems, while 12-bit absolute accuracy is unnecessary, 12-bit or higher resolution may be required; here, less accurate (and less costly) bandgap references may be used.

Q. What do you mean by "buried Zener" and "bandgap"?

A. These are the two commonest types of precision references used in integrated circuits.

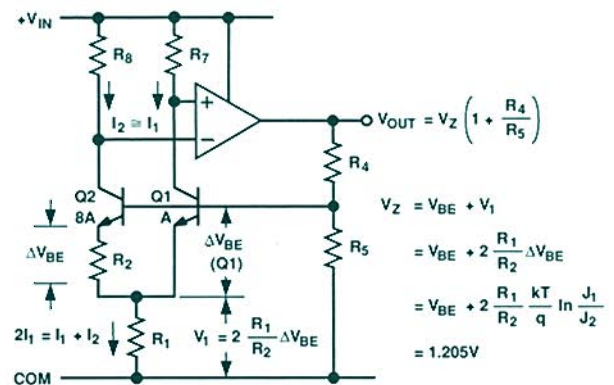
The "buried" or subsurface Zener is the more stable and accurate. It consists of a diode with the correct value of reverse-breakdown voltage, formed below the surface level of the integrated-circuit chip, then covered by a protective diffusion to keep the breakdown below the surface.



At the surface of a silicon chip there are more impurities, mechanical stresses and crystal-lattice dislocations than within the chip. Since these contribute to noise and long-term instability, the buried breakdown diode is less noisy and much more stable than surface Zeners—it is the preferred on-chip reference source for accurate IC devices.

However, its breakdown voltage is normally about 5 V or more and it must draw several hundred microamperes for optimum operation, so the technique is not suitable for references which must run from low voltage and have low power consumption. For such applications, the "bandgap" reference is preferred. It develops a voltage with a positive temperature coefficient to compensate for the negative temperature coefficient of a transistor's V_{be} , maintaining a constant "bandgap" voltage. In the circuit shown,* Q2 has 8 times the emitter area of Q1; the pair produces a current proportional to their absolute temperature (PTAT) in R1, developing a PTAT voltage in series with the V_{be} of Q1, resulting in a voltage, V_Z , which does not vary with temperature and can be amplified, as shown. It is equal to the silicon bandgap voltage (extrapolated to absolute zero).

Bandgap references are somewhat less accurate and stable than the best buried-Zener references, but temperature variation of better than 3 ppm/°C may be achieved.



Q. What precautions should I take when using voltage references?

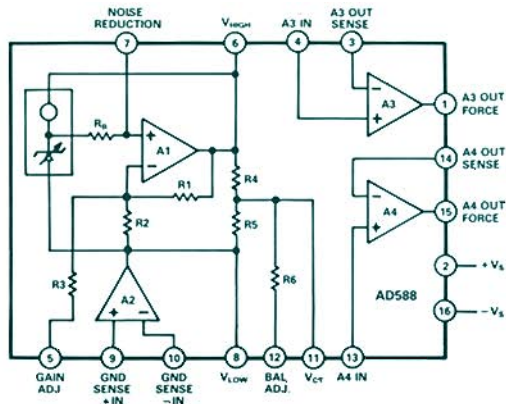
A. Remember the basics of good analog circuit design: beware of voltage drops in high impedance conductors, noise from common ground impedances, and noise from inadequately decoupled supply rails. Consider in which direction the reference current is flowing, and be careful of capacitive loads.

Q. I know about the effects of voltage drop and noise, but do references have to supply large-enough currents for voltage drop in conductors to be significant?

A. Generally, references are internally buffered; most will source and sink 5-10 mA. Some applications may require currents of this order or greater; an example is where the reference serves as the system reference; another is in driving the reference input of a high speed flash ADC which, has very low impedance. A current of 10 mA flowing in 100 mΩ will experience a voltage drop of 1 mV, which may be significant. The highest-performance voltage references, such as the AD588 and AD688, have Kelvin (force-sense) connections for both their output and output ground terminals. By closing a feedback

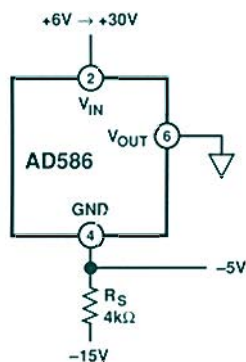
*From *Analog Dialogue* 9-1 (1975) also *The Best of Analog Dialogue*, 1967 to 1991, p. 72.

loop around the sources of error, these connections avoid the effects of voltage drops; they also correct gain and offset errors when current-buffer amplifiers are used to drive substantial loads or sink currents flowing in the wrong direction. The sense terminal should be connected to the output side of the buffer amplifier, preferably at the load.



Q. What do you mean by “flow in the wrong direction”?

A. Consider a +5-V reference operated from a +10-V supply. If its 5-volt output terminal is loaded by a resistor to ground, current will flow out of the terminal. If the resistor is instead connected to the +10-V supply, current will flow into the terminal. Most references will allow net current flow in either direction; but some will source current but not sink it—or will sink much less than can be sourced. Such devices, identifiable by the way their output current is specified on the data sheet, may not be used in applications where substantial net current must flow into the reference terminal. A common example is the use of a positive reference as a negative reference.



Q. Why not just buy a negative reference?

A. Because most single voltage-output references are positive references. Two-pin active references, of course, can be used for either polarity; they are used in the same way as Zener diodes (and they are usually bandgap devices).

For a three-terminal positive reference to be used as a negative reference, it must be able to sink current. Its output terminal is connected to ground and its ground terminal (which becomes the negative-reference terminal) is connected to the negative supply via a resistor (or a constant current source). The positive supply pin must generally be connected to a positive supply at least a few volts above ground. But some devices can provide negative reference in the two-terminal mode: the positive and output terminals are connected together to ground.

R_S (or a current source) must be chosen so that for all expected values of negative supply and reference load current the ground- and output-terminal currents are within ratings.

Q. What about capacitive loads?

A. Many references have output amplifiers that become unstable and may oscillate when operated with large capacitive loads; so it is inadvisable to connect high capacitance (several μF or more) to the output of a reference to reduce noise, but 1-10 nF capacitors are often recommended—and some references (e.g., AD588) have noise-reduction terminals to which capacitance can be safely connected. If force-sense terminals are available, it may be possible to tailor loop dynamics under capacitive load. Consult data sheets and manufacturers’ Application Engineers to be sure. Even if the circuit is stable, it may not be advisable to use large capacitive loads since they increase the turn-on time of the reference.

Q. Don’t references turn on as soon as power is applied?

A. By no means. In many references the current that drives the reference element (Zener or bandgap) is derived from the stabilized output. This positive feedback increases dc stability but leads to a stable “off” state that resists startup. On-chip circuitry to deal with this and facilitate startup is normally designed to draw minimal current, so many references come up somewhat slowly (1-10 ms is typical). Some devices are indeed specified for faster turn-on; but some are even slower.

If the designer needs reference voltage very quickly after power is applied to the circuit, the reference chosen must have a sufficiently fast turn-on specification; and noise reduction capacitance should be minimized. Reference turn-on delay may limit the opportunities for strobing the supplies of data conversion systems in order to conserve system power. The problem must still be considered even if the reference is built into the converter chip; it is also important in systems of this type to consider the power-up characteristics of the converter as well [discussed in “Ask the Applications Engineer—1,” *Analog Dialogue* 22-2 (1988), p. 29].

High-precision references may require an additional period of thermal stabilization after turn-on before the chip reaches thermal stability and thermally induced offsets arrive at their final values. Such effects will be mentioned on the data sheet and are unlikely to exceed a few seconds.

Q. Does using these high precision references instead of its internal reference make a converter more accurate?

A. Not necessarily. For example, the AD674B, a high-speed descendant of the classical AD574, has a factory-trimmed calibration error of 0.25% (± 10 LSB) max, with an internal reference guaranteed accurate to within ± 100 mV (1%). Since 0.25% of 10 V = 25 mV, full scale is 10.000 V ± 25 mV. Suppose that an AD674B with a 1%—high internal reference (10.1 V) had been factory-trimmed for 10.000 V full scale, by a 1% gain increase. If an accurate 10.00-V AD588 system reference were to be connected to the device’s reference input, full scale would become 10.100 V, at 4 times the specified max error.

Q. Please discuss the role of the clock as a system reference.

A. Oops, we’re out of space! This question introduces a topic that merits thoughtful discussion. We’ll do it in a future issue. ▀

Worth Reading

DATABOOKS

1992 Data Converter Reference Manual (*Two volumes, 3,232 pages*). Vol. 1: DACs, S/D converters, Communications products, DPMs, DSP products, Bus interface and serial I/O products, ASICs. Vol. 2: ADCs, V/F and F/V converters, Sample/track-hold amplifiers, Switches & muxes, Voltage references, Data-acquisition subsystems, Analog I/O ports, ASICs. **FREE. Circle 26**

1992 Audio/Video Reference Manual (*104 products, 42 application notes, 1,216 pages*). Includes op amps, Audio ADCs, Video ADCs, Audio DACs, Video DACs, Special-function audio products, Special-function video products, DSP products, Other products, Application notes. **FREE. Circle 27**

GUIDES

1992 Amplifier Applications Guide: 648 pages of timely and practical information on amplifiers—including operational, audio, instrumentation, video, and log amps. Topics include: Introduction; Precision Transducer Interfaces; High-impedance, low current; Single-supply, low power; Audio; Filtering, Driving ADCs; Video and other high-speed applications; Nonlinear circuit applications; Unusual applications; Subtleties; Hardware techniques; Simulation; and a complete Index. Notes for the 1992 Seminar Series, written by the Applications Engineering staff of Analog Devices and edited by Walt Kester. *Price is only \$20.* Use the book order card.

Multiple Digital-to-Analog Converter Integrated Circuits: 32-page Selection Guide. Covers 8-12-14-16-18-bit duals, 6-8-10-bit triples, 8-12-14-bit quads, 8-12-bit octuples. **Free. Circle 28**

Instrumentation Amplifier Application Guide by Charles Kitchin and Lew Counts. 44 pages. Basic instrumentation-amplifier theory; Design considerations for in amps; In-amp applications. Appendixes: In-amp specifications; Monolithic in amps available from Analog Devices. **Free. Circle 29**

SERIAL PUBLICATION

DSPatch—The DSP Applications Newsletter: Number 22, Winter, 1992, 20 pp. Featuring a new EZ-Lab—the ADSP-21020 [floating-point] Evaluation Board—and a complete guide to third-party DSP products. Also featuring an Alcatel AG G.722 telephone; a DSPG Ltd. ADSP-2101-based implementation of the 06 series speech codec for GSM; Galysh Enterprise CTC16dsp model-railroad control system; Radius PowerView™ display interface for Macintosh PowerBook™ computers; Computer Continuum's LAB-DSP board; Independent Digital Consulting's ID2105EM low-cost emulator for the ADSP-2105; products from Hollis Electronics, Innovative Devices, Signalogic, Quantawave; New DSP packages for Universities; and much more. **Circle 30**

APPLICATION NOTES

Using the AD834 [ultrafast 4-quadrant analog multiplier] in DC to 500-MHz applications: RMS-to-DC conversion, Voltage-controlled amplifiers, and Video switches, by Mark Elbert and Barrie Gilbert (AN-212), 12 pages. **Circle 31**

Video VCAs and Keyers using the AD834 and AD811, by Eberhard Brunner, Bob Clarke, and Barrie Gilbert. (AN-216), 8 pp. **Circle 32**

Digital control system design with the ADSP-2100 family, Kapriel Karagozian, 12 pp. AN-227 **Circle 33**

REPRINT AVAILABLE

ADC achieves 12-bit resolution at 25.6 Msamples/s, by David Duff, *Microwaves & RF*, July, 1991. About AD9032. **Circle 34**

MINI BOOK REVIEW

Analog Circuit Design—Art, Science, and Personalities, edited by Jim Williams. Boston: Butterworth-Heinemann, 1991.

This unusual engineering book combines history, philosophy, and design, expressed in 30 free-ranging chapters written individually by a group of design luminaries at the invitation of Editor Jim Williams. He placed no boundaries on length, content, or style, just required that there be a connection to the world of analog circuit design. His motive was to expose the reader to a wide range of design approaches, hoping that common themes of successful design would emerge. This goal has largely been met.

We find that there is some science and some art, but underlying it all is a solid understanding of the fundamentals—feedback theory, physics, and a methodical approach to troubleshooting. An experienced designer's unique style emerges as a result of one's motivations, history of personal development, self-knowledge (strengths and weaknesses), when to ask questions, and when to believe the answers. Learning about designers and the variety of their styles and backgrounds through their own stories will help the budding would-be designer choose a path.

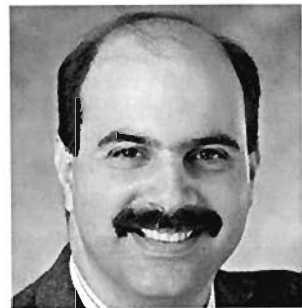
The 22 authors' offerings divide into 5 sections: Introduction; What is analog design? The making of an Analog Engineer; Intuitions and insights; and Techniques, tips, and applications.


The contributors have demonstrated the ability to choose a "best" design approach to analog circuit design problems. Most have developed commercially successful products or elegant circuits. Their stories have valuable lessons for all design engineers; this book belongs on every analog designer's bookshelf. When circuits won't behave, remember that the industry's luminaries have had similar problems. And "There is always A Way Out."

Doug Grant 

MORE AUTHORS (Continued from page 2)

Adolfo A. Garcia (page 18), is a Staff Applications Engineer for the PMI Division of ADI in Santa Clara, CA. He has written articles, application notes, and Design Ideas for publication and developed SPICE models for op amps and non-linear analog circuits. Earlier, Adolfo did design engineering at Avantek, Ford Aerospace, and Hughes Aircraft. Adolfo holds a BSEE from Santa Clara University and a MSEE from UCLA. In spare time, he coaches baseball and enjoys fine dining, bicycling, billiards, & Corvettes.



James Bryant (page 20) is European Applications Manager for ADI, based in Walton-On-Thames, England. His photo and a biographical sketch appeared in *Analog Dialogue* 25-1. 

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

NEW AND REVISED DATA SHEETS ••• A pin- and code-compatible 16-MHz version of the ADSP-2101 is now available—the ADSP-2101-66§ ••• A new data sheet is available for the ADSP-2100 family In-Circuit Emulators (ADDS-21XX-ICE); it includes the ADDS-2111-ICE Emulator† ••• A data sheet (ADDS-2111-EZ) is available for ADSP-2111 EZ Development Tools ¶ ••• AD9003A is a pin-compatible replacement for AD9003, at much lower cost** ••• The AD664 monolithic quad 12-bit DAC is now available in 28-pin plastic DIP and 44-pin PLCC. A die revision has resulted in improved digital timing, and other improvements†† ••• The AD645 low-noise amplifier has improved drift specifications. Grade C is 1 $\mu\text{V}/^\circ\text{C}$, and grades A and B have been improved to 5- and 2 $\mu\text{V}/^\circ\text{C}$, respectively§§.

ERRATA ••• In *Analog Dialogue* 25-2, page 8, the EZ-LAB Evaluation Board design team included Chris Caviglioli (JTAG controller and PC & RS-232 interface) ••• In the *Audio/Video Reference Manual*, AN-216, p. 11-193 ("Video VCAs and keyers using the AD834 and AD811"), Resistor R9 was omitted from Figure 1. R9 is connected between analog ground and the + input of U3. The error has been corrected in the separately printed version of AN-216†. In AN-212, p. 11-151 ("Using the AD834 in dc to 500-MHz applications"), Figure 3, the 0.01 μF capacitors can be 0.022 μF (in the two paragraphs below eq. (3), they should be referred to as 22 nF, not 22 μF). The same mistake exists in the separately printed version of AN-212 ••• AD1154 data sheet: mechanical outline is changed to reflect a change from metal platform DIP to hermetic ceramic DIP package. Model numbers AD1154AD/BD replace AD1154AW/BW. CWYLSO*.

PRODUCT NOTES (CWYLSO* for details) ••• AD586LR version of the AD586 precision 5-V reference is introduced, with initial error of 2.5 mV and 5 ppm/ $^\circ\text{C}$ drift ••• Because of our acquisition of PMI, there are currently two independent sources for 7524 DACs within Analog Devices, the AD7524 (Ireland) and the PM-7524 (California). No need to go elsewhere for second-source devices ••• DAC-8412/13 is now available in production quantities in plastic DIPs and PLCCs ••• Pin-compatible HDS-1250A replaces the HDS-1250 DAC, with some spec changes ••• AD2XX series interface products AD230, AD232, etc.) should be connected exactly as shown on the data sheet; in particular, the capacitor on the V+ terminal must be connected to V_{CC}, not ground ••• The AD7874 THD and peak harmonic specs (A and S grades only) have been changed to -78 dB ••• The ADSP-21000 Family C Compiler and Runtime Library give you the option of programming floating-point systems in C. Available for IBM-compatible PCs and Sun 4 workstations ••• A Design Idea note is available for low-cost digital soundfield (or "hall" effect) with the SSM-2125 Dolby Prologic Decoder. CWYLSO*

MILITARY, HI-REL, AND STANDARDS (CWYLSO* for details) ••• The AD689 precision 8.192-V reference is now available in SQ and TQ/883 versions (4-mV offset, 10-ppm/ $^\circ\text{C}$ drift for the TQ) ••• Our Analog Devices Semiconductor facility in Wilmington MA has been certified by DESC for the manufacture of Class S wafers for JAN devices ••• Analog Devices B.V., in Limerick, Ireland, successfully passed the certification audit for ISO9001, the most stringent and comprehensive of the ISO standards, and will receive an ISO9000 registration.

SHOWS, BBS, COMMUNICATIONS, etc. ••• Among the shows we will be exhibiting at later in 1992: DISKCON '92, San Jose, CA, Sept. 23-24; AES '92, San Francisco, CA, Sept. 28-Oct. 1; Sensors Expo '92, Rosemont, IL, Sept. 29-Oct. 1; Japan Audio Fair '92, Tokyo, Oct. 9-13; Japan Electronics Show '92, Osaka, Oct. 19-21; Convergence '92, Dearborn, MI, Oct. 19-21, Electronica '92, Munich, Germany, Nov. 10-14. If you're in the neighborhood, come see us ••• Fixed-point DSP workshops ("System Programming and Development with the ADSP-2100 Family") will be held in Norwood MA, June 10-12 and September 9-11. Send for Bulletin M1274‡‡ ••• DSP Bulletin Board: source code for many popular signal-processing algorithms using the ADSP-21020 floating-point chip are now available on the BBS. Set your modem to 8 data bits, 1 stop bit, no parity, 300/1200/2400 baud, and call (617) 461-4258. New users validated on Wednesdays ••• US Applications Hot Line: 1-800-ANALOGD—call any time; talk to a live applications engineer between 8:00 AM and 8:00 PM, Eastern Time ••• New SPICE Model (since ADSpice Release E): AD843 34-MHz fast-settling op amp. For info, call (408) 562-7206 or FAX (408) 727-1550 ••• Standard ADSP-2100 and ADSP-21000 families DSP University Packages are available at invitational prices for university professors who are teaching or doing research on projects involving DSP. CWYLSO*

PATENTS AND TRADEMARKS ••• New trademark: TrimDAC® ••• 5,043,295 by Paul Ruggerio and Cynthia Anderson for Method of forming an IC chip with self-aligned thin-film resistors ••• 5,065,144 by Steven Edelson, Gary Frattarola, and George Heron for Apparatus and mix-run encoding of image data ••• 5,070,331 by Shinichi Hisano for High-resolution d/a converter operable with single supply voltage ••• 5,077,541 by Barrie Gilbert for Variable-gain amplifier controlled by an analog signal and having a large dynamic range ••• 5,086,370 by John Yasaitis for Integrated circuit chip formed with a capacitor having a low voltage coefficient, and method of making such capacitor.

IN THE LAST ISSUE

Volume 25, Number 2, 1991, 28 Pages

For a copy, circle 38.

Editor's Notes, Authors

ADSP-21020 Floating-Point DSP:

Floating-point DSP chip for high-speed signal processing

Numerical C speeds code development and execution

Development tools and third-party support for floating-point DSP

Single-supply in-amp for automotive applications (AD22050)

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3 new single- and multichannel S/H chips (AD9100, AD682, SMP-18)

Monolithic 10-bit, 18-MSPS sampling ADC with on-chip T/H (AD773)

Complete 16-bit SOIC DACPORT™ includes on-chip 10-V ref (AD669)

New-Product Briefs:

Serial DACPORTs™ in 12-bit DIPs and SOICs (AD7233/7243)

8 12-bit MDACs on a chip with serial input, +5-V supply (AD7568)

Dual 18-bit audio DAC: 107-dB SNR, 16 \times oversampling (AD1865)

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Sampling ADC: 16-bit 100-kSPS, serial, autocalibrated (AD1876)

12-bit 750-kSPS sampling ADC dissipates <350 mW (AD7886)

Flexible 12-bit, 8-10- μs ADCs:

Improved performance for \times 74 sockets (AD774B)

Low cost, low power, small package (ADC-912A)

Advanced SPICE op-amp macromodel: a powerful tool for designers

Analog Devices names two new Fellows: Derek Bowers and Wyn Palmer

Ask the Applications Engineer—10: *When is a wire not a wire?*

Worth Reading

Potpourri (Last Issue, Errata, Product Notes, Updates, Patents)

Advertisement

*CWYLSO: Check with your local Analog Devices sales office.

†Circle 35 ... §Circle 39 ... ‡Circle 40 ... ¶Circle 41 ... **Circle 42 ... ††Circle 43 ... §§Circle 44 ... ‡‡Circle 45

For everyone who's tried to copy our AD574, here's your assignment for the next ten years.

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The AD1674 retains the pinout and functionality of the AD574, AD674 and AD774, while integrating a high-bandwidth sample/hold circuit, higher speed, lower power, and lower price - from \$14.15 (suggested, 100s). The AD1674 accepts input signals of $\pm 5V$, $\pm 10V$, $0-10V$ or $0-20V$, while operating from its standard 10V on-chip voltage reference (available for driving external loads).