AN1288: Si828x External Enhancement Circuits

The Si828x isolated gate drivers fulfill the demands of many high voltage power applications. The Si828x have robust gate drive capability and protection circuits that maximize system efficiency and ensure reliable operation.

For larger systems that require very large or multiple parallel switching devices and for systems (such as SiC FET) that operate at a high switching speed, additional circuits comprised of low-cost external components can extend the Si828x capabilities many ways. For example, it is possible to increase the effective output current to drive larger SiC FET/IGBT modules or to adapt the Si828x to drive and protect higher switching speed SiC FET devices.

This application note discusses circuit enhancements and their associated performance improvements, including a current drive booster which will increase gate current drive above 20 A, circuitry for reducing DESAT protection response time below 1 µs while maintaining robust noise immunity, a DESAT threshold adjustment which enables a threshold below the nominal 7 V, a method of adjusting the soft shutdown time in the event of a fault, and an external enhancement of the internal Miller clamp, improving the suppression of the Miller spike which can occur when the external transistor is turned off.

KEY FEATURES

- Current drive above 20 A
- DESAT protection response time < 1 µs
- DESAT threshold adjustment
- Adjustable soft shutdown current to minimize VDS voltage spikes or to minimize shutoff time
- External Miller clamp

1. Introduction

The Si828x family (Si8281/82/83/84/85/86) is made up of isolated, high-current gate drivers with integrated system safety and feedback functions. These devices are ideal for driving power SiC FETs and IGBTs used in a wide variety of inverter and motor control applications. A dedicated DSAT pin detects the desaturation condition and immediately shuts down the driver in a controlled manner. The Si828x devices also integrate a Miller clamp and negative VSSB to secure the power switch in the off state.

2. Enhanced Gate Drive Current

2.1 Standard Gate Drive Capability

In the following figure, we see a driver with no enhancements. RH = RL = 0 Ω, and typical source current is about 3 A:

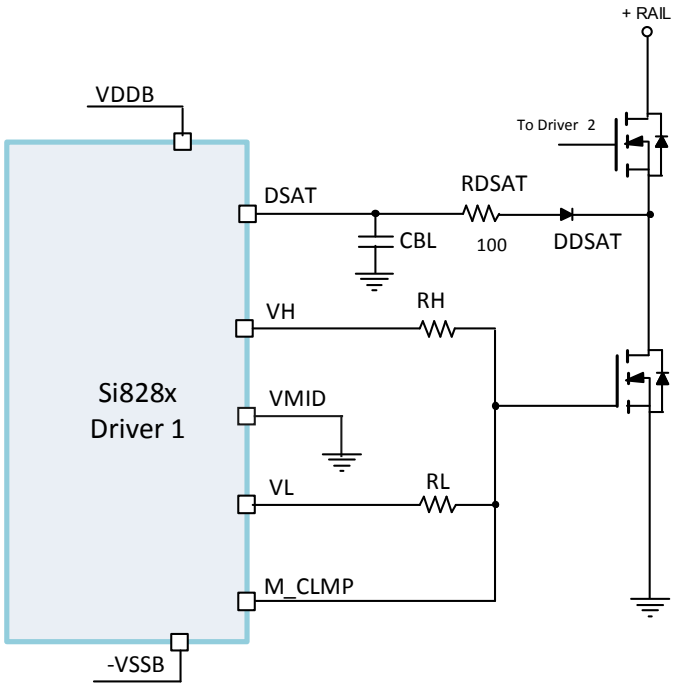

Figure 2.1. Standard Gate Drive Circuit

The following figure shows typical sink current of about 6 A:

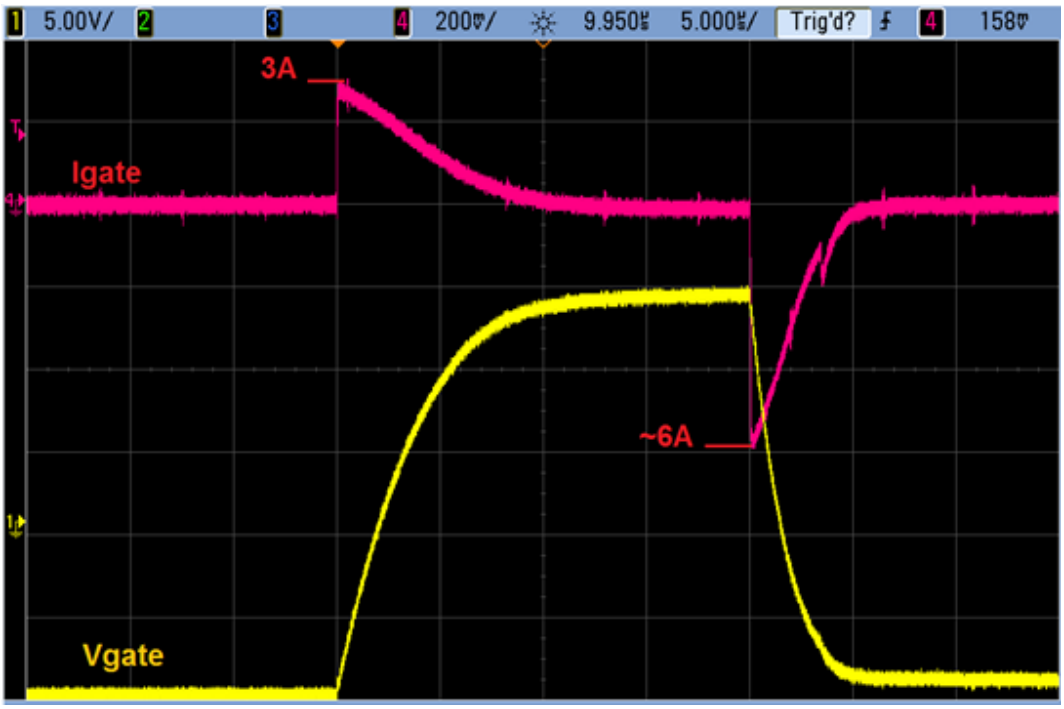

Figure 2.2. Standard Gate Drive Circuit Response with 220 pF Gate Capacitor

2.2 Si828x with Current Booster Circuit (Q1: FZT951, Q2: ZXTN2010)

The figure below depicts an example drive enhancement circuit for the Si828x. Q1 and Q2 bipolar transistors provide enhanced drive current controlled by VH and VL, respectively. Each base has a current limiting resistor, and there is a diode between VH and VL to assist in turning off Q1 and Q2 at the appropriate time. Gate resistors RH and RL are connected to the emitter circuits of Q1 and Q2, respectively.

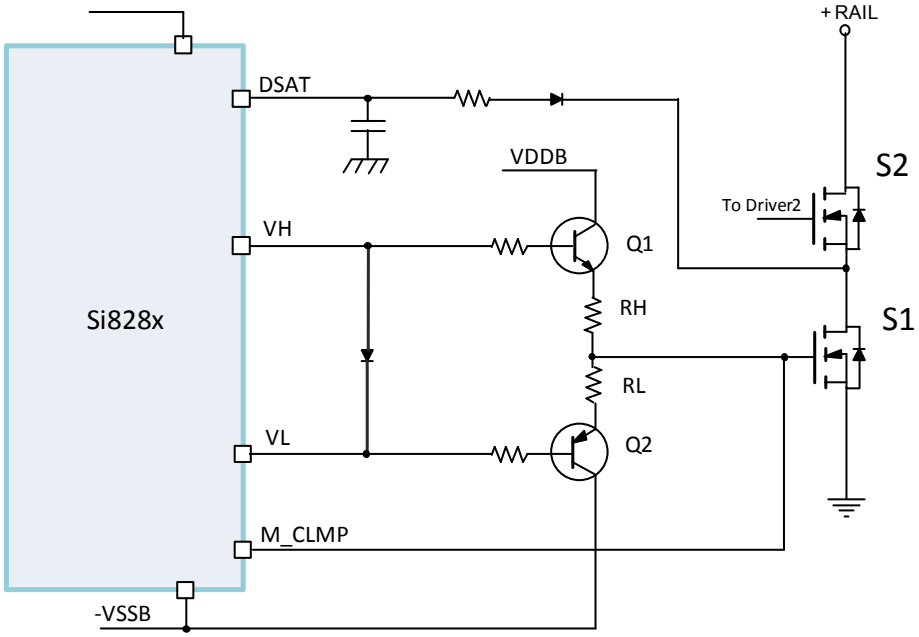

Figure 2.3. Si828x with Current Booster Circuit (Q1: FZT951, Q2: ZXTN2010)

In the figure below, we see a significantly improved gate drive response in contrast to that shown in Figure 2.2 Standard Gate Drive Circuit Response with 220 pF Gate Capacitor on page 3, with peak source current of 20 A and peak sink current of 30A. In this case, RH = RL = 0 Ω.

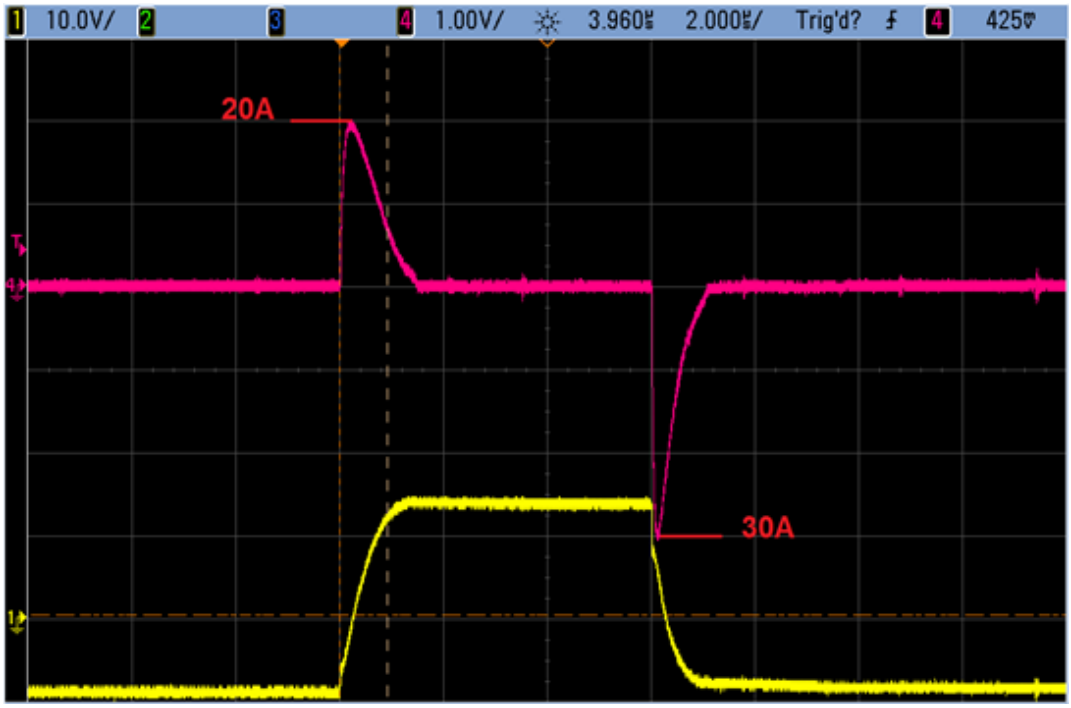

Figure 2.4. Si828x Gate Drive Response with Current Booster Circuit (Q1: FZT951, Q2: ZXTN2010)

2.3 Si828x with Current Booster Circuit (PHPT60415NY/ PHPT60415PY)

The user has options in the choice of driver transistors but may see different performance. If we substitute transistors PHPT60415NY and PHPT60415PY for FZT951 and ZXTN2010 seen in the previous circuit, we observe a different gate drive response. In this case, both source current and sink current are now observed to be 14A each. Nevertheless, clearly gate current is highly dependent on the choice of Q1 and Q2 transistors (see Table 7.2 Booster Pair (Q1, Q2) Recommendations on page 23 for a list of Q1, Q2 recommendations). Once again, RH = RL = 0 Ω. See the following figure.

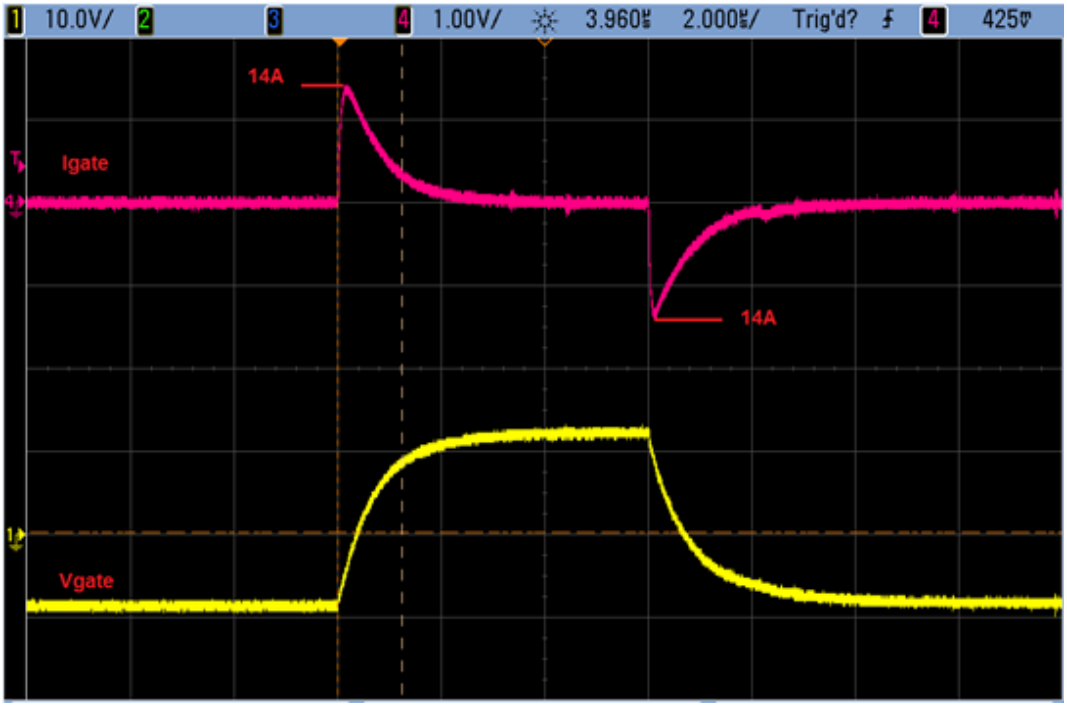

Figure 2.5. Si828x Gate Drive Response with Current Booster Circuit (PHPT60415NY/ PHPT60415PY)

3. Standard Overcurrent Protection for SiC FET and IGBT (DESAT and Soft Shutdown)

In an overloaded condition, commonly there is a very low impedance across the load (shown as an inductor short in the figure below). As a result, the current flow can increase more than 20 times the normal load current. This extremely high current causes the VCE and power dissipation of the IGBT to dramatically rise and the IGBT must be safely shut down to protect against damage. The Si828x DESAT protection circuit comprises a detection circuit and a soft shutdown circuit. The response time of these two circuits result in the total DESAT protection response time. With external components the DESAT protection response time can be customized to meet the specific requirements of different systems.

During a shorted load fault condition, the switch S1 turns on into a short with the full DC Rail connected right across C-E. In this case, the VCE is very large and the diode between the DSAT pin and the Collector has reverse bias and allows the DSAT pin voltage to ramp up freely (see 4.3 DESAT Protection Behavior with Threshold Adjustment in the Case of Overload (Zener Diode) for more information on this fault condition).

To detect this condition, the gate driver has a DSAT pin to sense the voltage across the IGBT and it will shut down the IGBT when the VCE voltage is larger than the DSAT Vth. Also included in the DESAT protection circuitry is an internal current source to charge the blanking capacitor CBL toward the voltage level across the IGBT. The internal current source is nominally 250 µA for the Si8286 and 1mA for the rest of the family. The speed of the detection timing is dependent on the value of the internal current source and the capacitor CBL.

The value of DESAT detection time is a tradeoff of the need for system level blanking (particularly when an external IGBT is first enabled) and the external transistor's thermal characteristics. DESAT detection time may need to be as fast as about 300 ns for SiC FETs and small MOSFET devices or can be as slow as 3 µs for thermally efficient IGBTs.

The standard gate driver over-current protection is shown in the following figure.

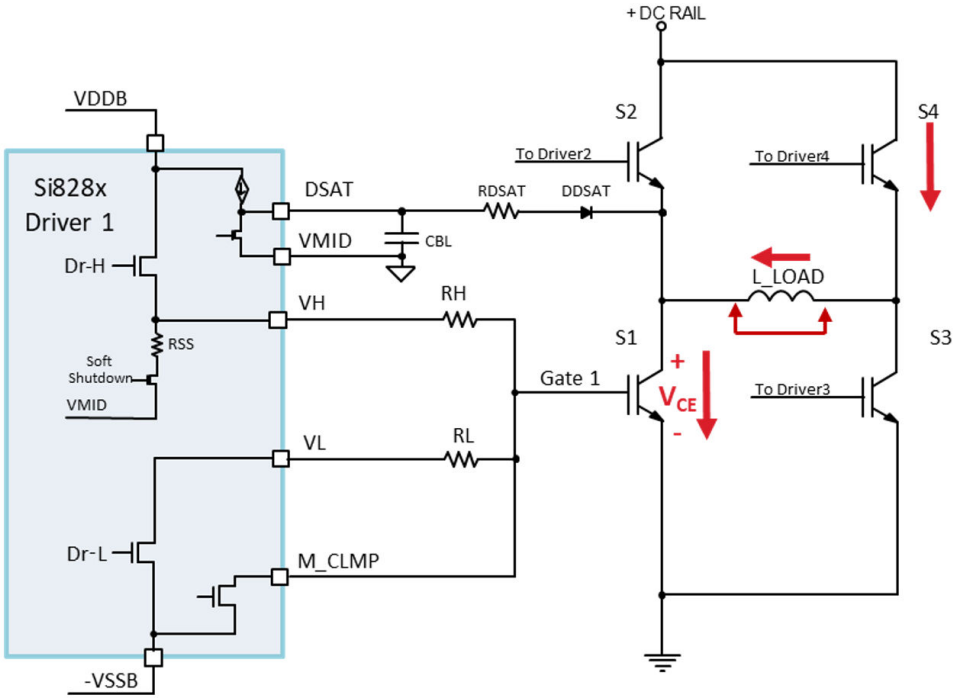

Figure 3.1. Standard Overcurrent Protection for SiC FETs and IGBT

3.1 Standard DESAT Protection Behavior

In normal operation, the PWM input IN+ goes high to drive the gate of S1 high. The signal Gate 1 rises to turn on S1. The DSAT pin begins to supply charging current to CBL at this point. As the drain voltage is quickly pulled low, the DSAT node is clamped close to ground through DDSAT and RDSAT, below Vth and no DESAT condition is reported.

The DESAT behavior with standard (internally set) DESAT threshold is shown in the figure below. When S1 is on, the low voltage on the collector normally causes CBL charging current to flow through DDSAT and thus the DSAT pin does not rise above the DESAT threshold. During an overload condition there is an increase in VCE. If VCE rising causes the DDSAT anode voltage to rise, the DSAT pin also rises. When the voltage at the DSAT pin reaches the internal DESAT threshold of 7 V, the IGBT or SiC switch device is considered to have gone into desaturation; once the threshold is crossed there is a short delay (shown as 0.5µs, Soft Shutdown time) before the Gate 1 signal is brought to -VSSB, turning off S1. The figure below displays behavior of the circuit found in Figure 3.1 Standard Overcurrent Protection for SiC FETs and IGBT on page 6. Note that the PWM pulse is 5 µs long, whereas the abbreviated gate pulse is 3 µs (detection time) due to the DESAT protection behavior.

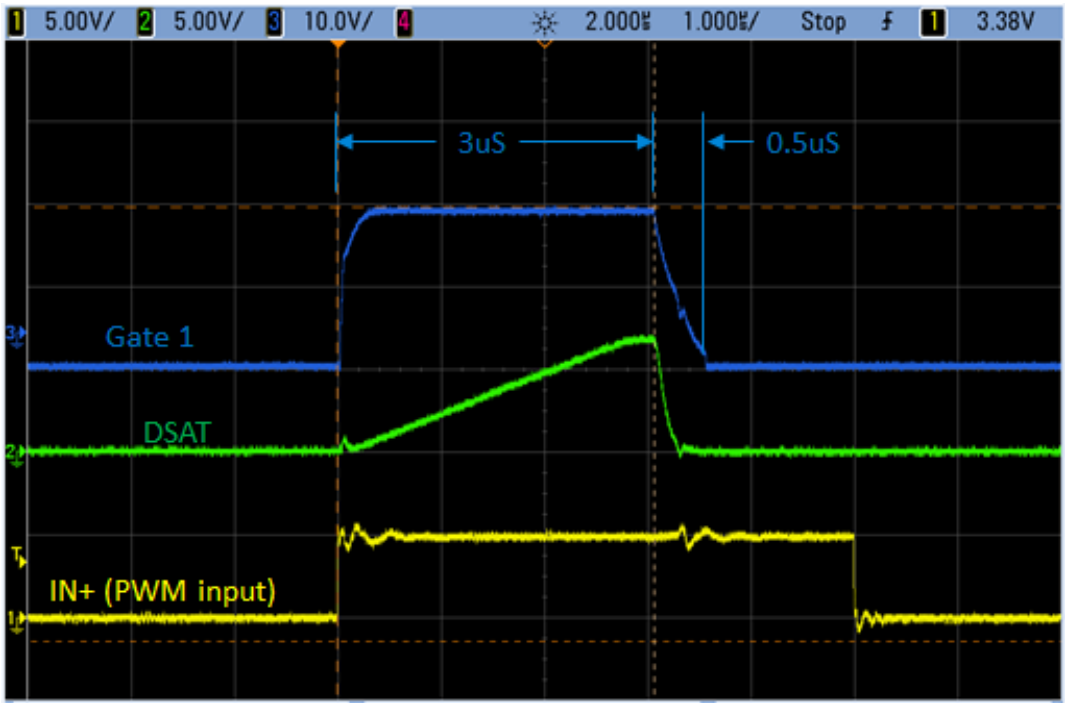

Figure 3.2. Signals for Standard Overcurrent Protection

3.2 Standard Internal Soft Shutdown

Standard Internal Soft Shutdown operates as follows: Once DESAT fault detection has occurred, driver transistors Dr-H and Dr-L are turned off and the Soft Shutdown MOSFET is turned on (MOSFET plus internal RSS series impedance is 50 Ohms). As a result, current flows *into* the VH pin and causes the Gate 1 voltage to ramp down toward -VSSB. Since the Soft Shutdown MOSFET has a much larger impedance compared to the VL driver (Dr-L, which is now off), the FET S1 is turning off more slowly than normal. As the Gate 1 signal falls, S1's drain current is switched off and eventually reaches zero current. The Soft Shutdown time of 0.5 µs appears relatively short in Figure 3.2 Signals for Standard Overcurrent Protection on page 7 because the gate capacitance of the test device is relatively small. Note that as S1's drain current goes from very high level (due to an overload or shorted drain condition) toward 0 A, the di/dt in this current ramp-down process will generate a VDS voltage spike. This voltage spike is minimized by the Soft Shutdown feature.

4. DESAT Threshold Adjustment: RDSAT, N Diodes/Zener

4.1 DESAT Protection Response Time < 1 µs with RI / Diode

Standard DESAT protection was discussed in section 3. Standard Overcurrent Protection for SiC FET and IGBT (DESAT and Soft Shutdown). The standard response time was shown to be about 3.5 µs. While 3.5 µs is sufficient to protect an IGBT from overcurrent-induced desaturation, SiC FETs require a much faster protection response to keep them safe.

To speed up the detection of the overload condition, it is not desirable to just reduce the value of CBL below 200 pF to prevent fault triggering as a lower-valued capacitor reduces noise immunity and is more vulnerable to noise coupling. However, it is more advantageous to add a resistor RI and a series diode between the VH and DSAT pins to speed up the charging of the CBL cap. This is an effective way to speed up the detection time without compromising the noise immunity of the DESAT circuit.

The additional current through RI = 2.2 k and DI to charge CBL = 270 pF reduces the total DESAT response time to 0.8 µs with 320 ns detection duration timing (see the following figure).

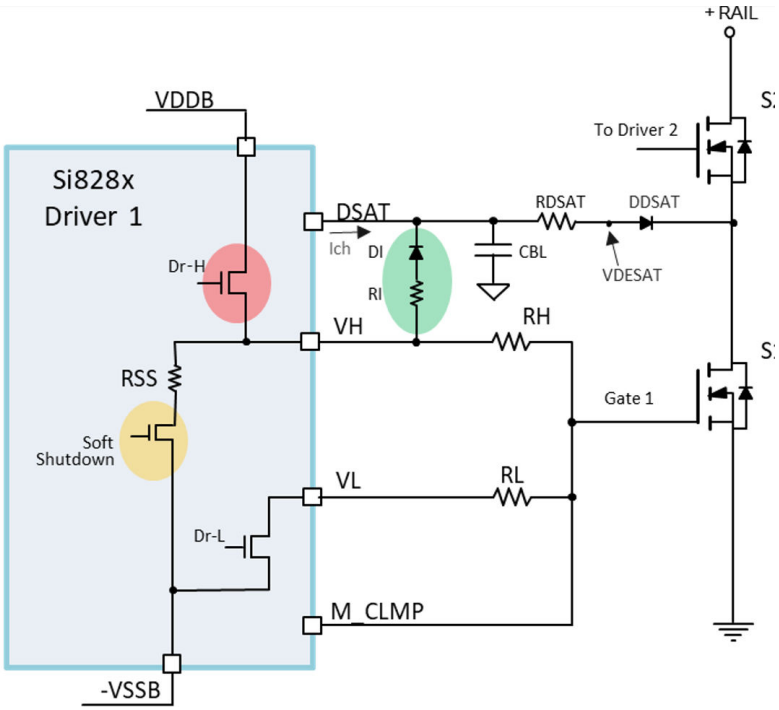

Figure 4.1. Si828x Enhanced Detection and Standard Internal Soft Shutdown

A simple equation may be used to calculate the DESAT protection response time when using the external RI and DI between the VH and DSAT pins:

$$t_{DESAT} = RI \times CBL \times In\left[\frac{Ich \times RI + VDDB}{Ich \times RI + VDDB - Vth}\right]$$

Equation 4.1. DESAT Protection Response Time with External RI

Where:

t_{DESAT} is the DESAT protection response time

RI is the value of the external resistor between VH and DSAT pins

CBL is the value of the external blanking capacitor at the DSAT pin

Ich is the current of the internal DESAT current source

VDDB is the voltage difference between VDDB and VMID

Vth is the DESAT threshold voltage

Example:

RI = 2.2 k

CBL = 270 pF

Ich = 1 mA (Si8285)

VDDB = 15 V

Vth = 7 V

$$t_{DESAT} = 2200 \times 270 \times 10^{-12} \times \ln\left[\frac{0.001 \times 2200 + 15}{0.001 \times 2200 + 15 - 7}\right] = 310ns$$

Equation 4.2.

The figure below illustrates this. As we can see, the Gate signal rises to its ultimate value of about 15V. VH has risen and begins to prepare the DSAT pin to detect the DESAT event by turning on the Ich current on the DSAT pin. The drain-to-source voltage of S1, VDS, begins to rise as drain current IDS rises in abnormal fashion well above the normal operating range. Rising VDS causes the DESAT diode to reverse bias, and all the current available from the DSAT pin and RI goes to charging CBL. From here, the DSAT pin voltage crosses the detection threshold quickly (here in 320 ns), disabling Dr-H and Dr-L and engaging the action of the Soft Shutdown transistor which pulls current from VH and the Gate node. The Gate node is drawn down toward -VSSB at a controlled rate, causing the device S1 to shut down over a period of about 980 µs. This timing is adequate for most SiC applications. However, for high performance applications with extremely good layout with low parasitic inductance, further optimization on soft shut down timing can provide faster response time as we will discuss in section 5. Adjustable Soft Shutdown. Moreover, faster DESAT soft shutdown generates larger voltage spike and designer needs to balance between faster response time and VDS voltage spike level.

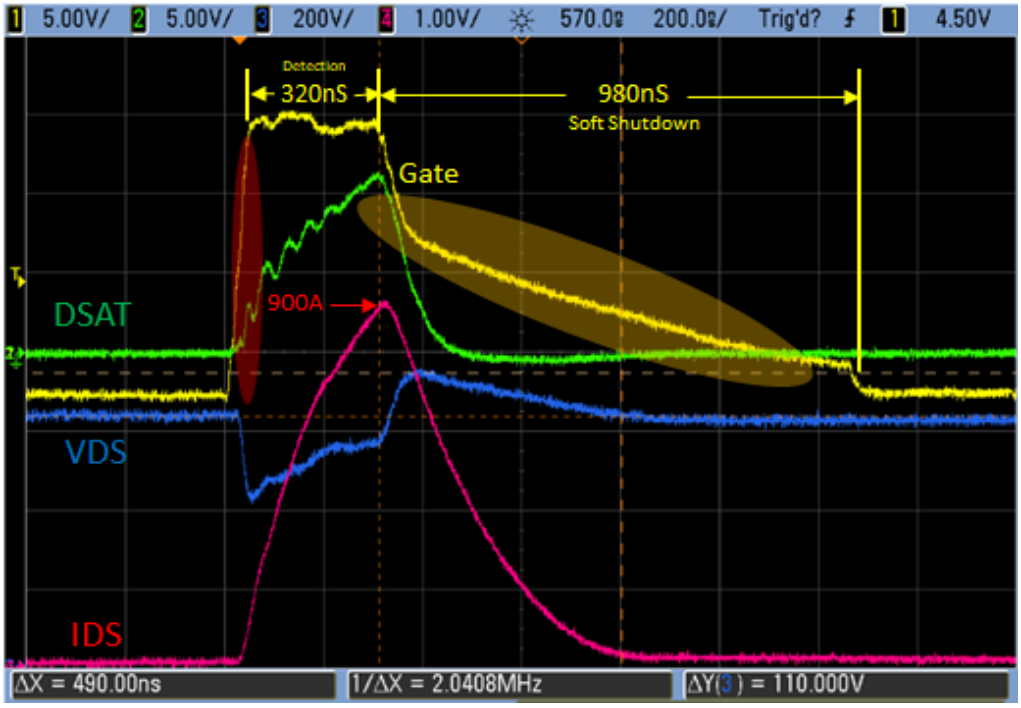

Figure 4.2. Signals for Enhanced Detection and Standard Internal Soft Shutdown

4.2 DESAT Protection Behavior with IDS Threshold Adjustment in the Case of Overload (Using RDSAT)

4.2.1 RDSAT without RI and DI

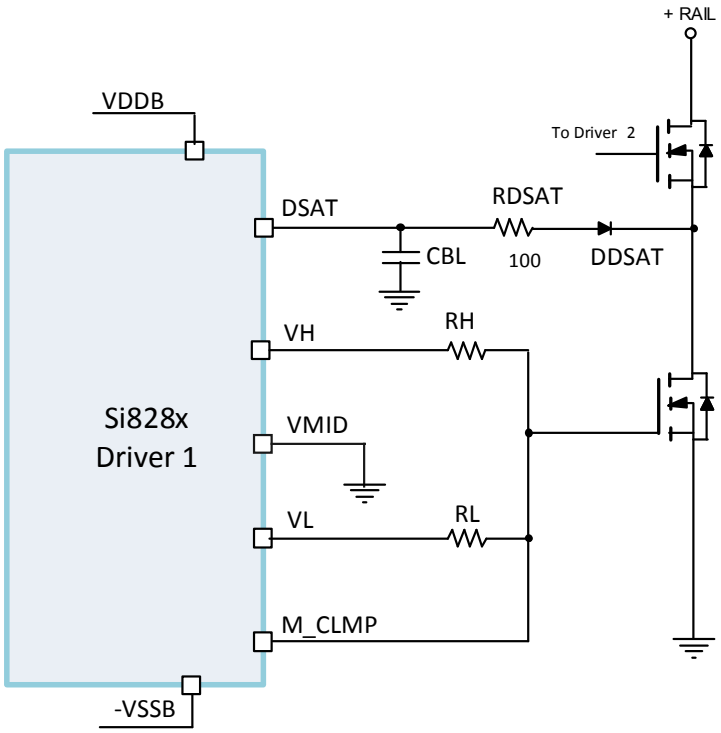

Figure 4.3. Standard Gate Drive Circuit

The value of RDSAT can be adjusted to control the IDS DESAT current level. Below is an equation to estimate the value of RDSAT.

$$RDSAT = \frac{(Vth - VDS - Vf)}{Ich}$$

Equation 4.3. RDSAT

Where:

Vth is the Si828x internal DESAT threshold.

VDS is the desired DESAT voltage

Vf is the diode forward voltage

Ich is the Si828x internal DESAT current source (250 µA for Si8286 and 1 mA for all others Si828x)

Example:

Target IDS DESAT current level: 350 A

From the SiC / IGBT data sheet: RDS (on) = 16 mΩ

Vf = 0.6 V

Ich = 1 mA (Si8285)

VDS at DESAT condition = IDS x RDS = 350 A x 16 mΩ = 350 x 0.016 = 5.6 V

RDSAT = (7 V – VDS - 0.6 V)/Ich = (7 – 5.6 – 0.6)/0.001 = 800 Ω

4.2.2 RDSAT with RI and DI

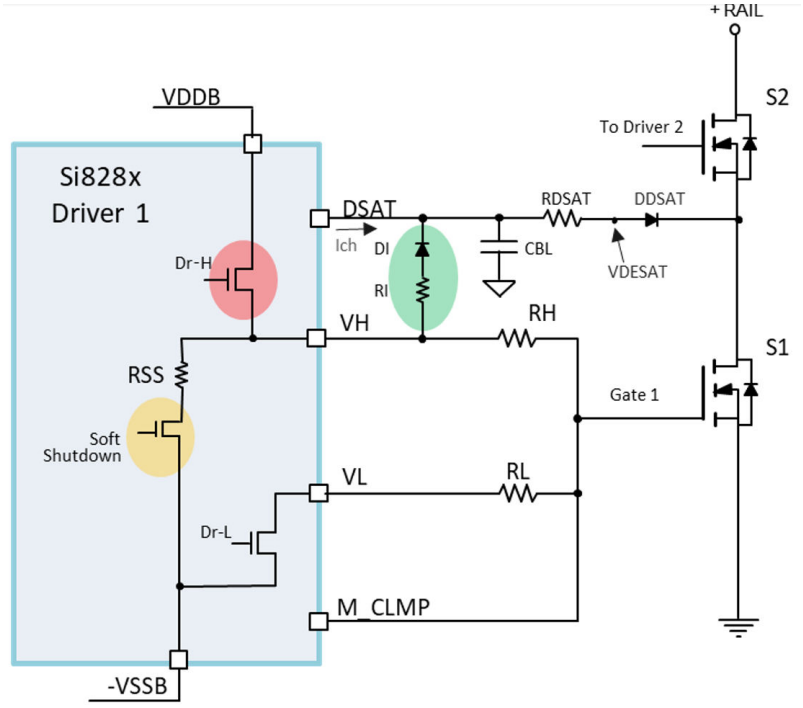

Figure 4.4. Enhanced Detection and Standard Internal Soft Shutdown

The value of RDSAT_E (enhanced) can be adjusted to control the IDS DESAT current level. Below is an equation to estimate the value of RDSAT_E:

Through current superposition

I_RI = (VDDB – 0.6 – Vth) / RI

I_RDSAT = Ich + I_RI

$$RDSAT\_E = (Vth - 0.6 - VDS) / I\_RDSAT$$

Equation 4.4. RDSAT_E

Where:

Vth is the Si828x internal DESAT threshold

VDS is the desired DESAT voltage

Vf is the diode forward voltage

Ich is the Si828x internal DESAT current source (250 µA for Si8286 and 1mA for all others Si828x)

Example:

Target IDS DESAT current level: 350 A

From the SiC/IGBT data sheet: RDS (on) = 16 mΩ

Ich = 1 mA (Si8285)

RI = 1.47 k

I_RI = (15 – 0.6 – 7) / 1,470 = 5 mA

I_RDSAT = 1 + 5 = 6 mA

VDS at DESAT condition = IDS x RDS = 350 A x 16 mΩ = 350 x 0.016 = 5.6 V

RDSAT_E = (7 V – 0.6 – 5.6) / I_RI = (7 – 0.6 – 5.6)/0.006 = 130 Ω

4.3 DESAT Protection Behavior with Threshold Adjustment in the Case of Overload (Zener Diode)

In the figure below, a 3.3 V Zener diode is inserted in the DESAT path, establishing a voltage drop in the sensing path thus reducing the SiC VDS DESAT triggering voltage level. The DESAT triggering voltage at DSAT pin is at 7 V. After the circuit modification, VDESAT = 7 V – 3.3 V = 3.7 V.

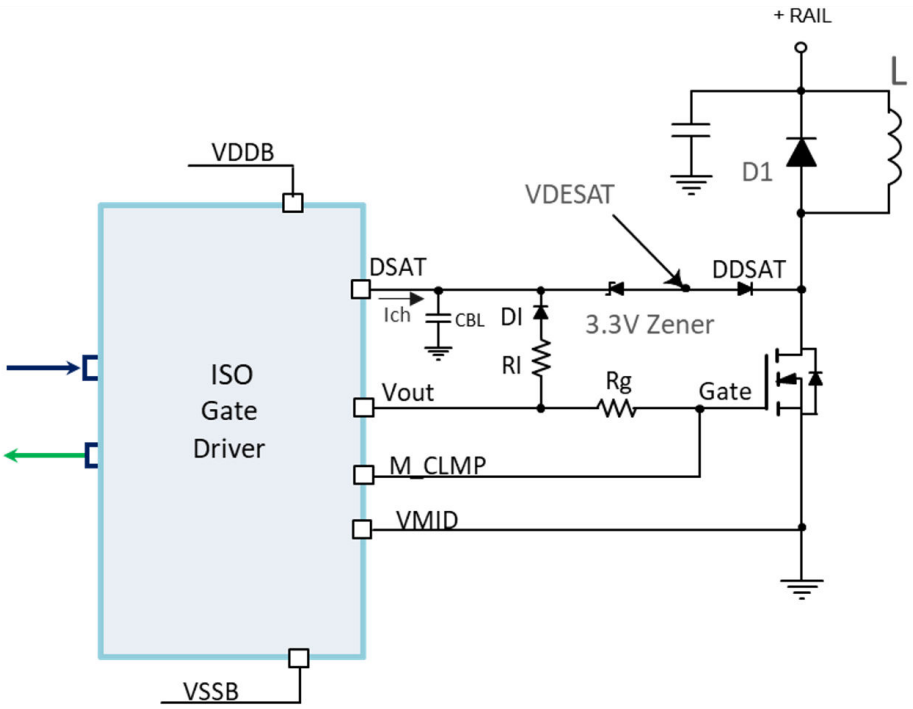

Figure 4.5. Circuit with DESAT Threshold Adjustment

The next figure shows the relative behavior of the DSAT pin and the VDESAT node and the impact on the gate node from the action of the reduced DESAT threshold. The first positive gate pulse causes the drain current and inductor current to increase and the drain voltage to rise, but the DSAT pin does not rise above the DESAT threshold. During the off time, flyback action due to continuous inductor current causes current to flow through SiC body diode D1 and drain current drops to zero. During the off state, the DESAT circuit is not active and the high VDS is not being monitored. The second gate pulse occurs when the inductor current has decayed slightly but is close to what it was when the switch was turned off. The switch once again causes the drain current and inductor current to rise and causes VDS to rise. VDS rising engages the DESAT protection mechanism, turning the switch device off. The drain current when DESAT protection is engaged is still high but only 50 A, less than the maximum drain current in the unadjusted case.

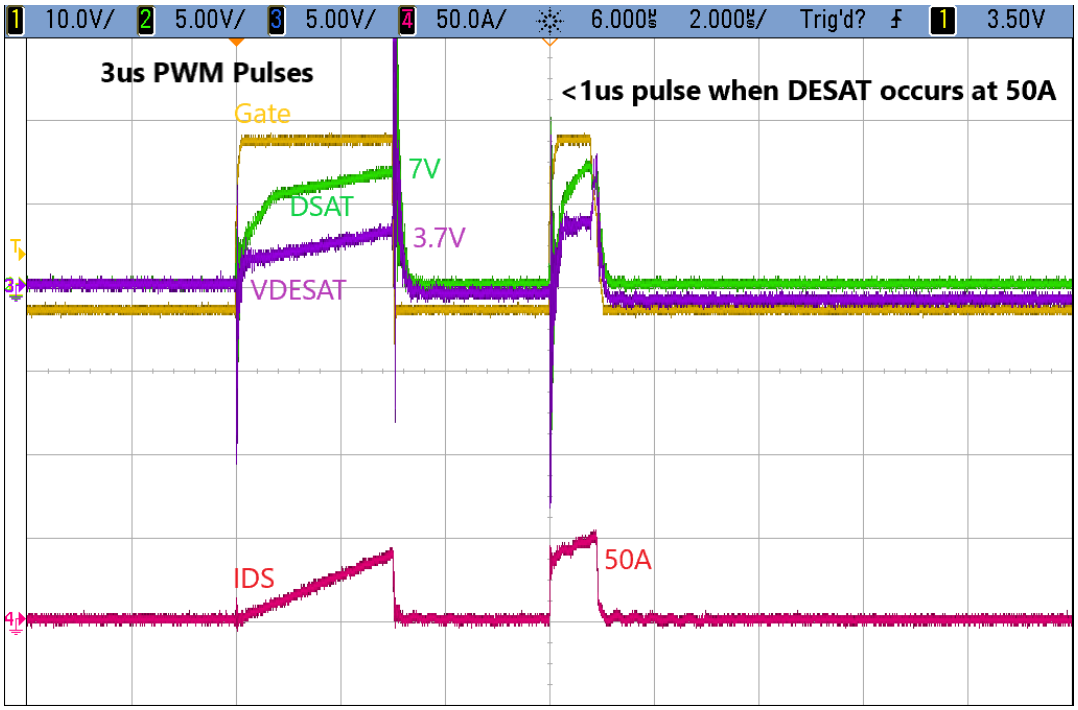

Figure 4.6. DESAT Threshold Adjustment Response

4.4 DESAT Protection Behavior with Threshold Adjustment in the Case of Shorted Load (with Zener Diode or RDSAT)

In the case of a shorted load, the drain of the SiC FET is at +DC-Rail potential, already well above the DESAT threshold of the Si828x when the SiC FET is turned on. As a result, the series diode DDSAT will not conduct and the series Zener diode will not produce a voltage drop which would reduce the DESAT threshold as in the case of overload discussed in 4.3 DESAT Protection Behavior with Threshold Adjustment in the Case of Overload (Zener Diode). However, the DESAT protection mechanism still operates based on the internal DSAT threshold: when VH is driven high, the internal Ich current source is turned on, charging blanking capacitor CBL. The high state of VH also results in additional charging current into CBL through RI (from 4.2 DESAT Protection Behavior with IDS Threshold Adjustment in the Case of Overload (Using RDSAT)), causing the CBL voltage to rise faster. When the voltage across CBL reaches the Si828x internal DESAT threshold, the DESAT mechanism activates. This results in turning off the VH drive transistor and the VL drive transistor. At the same time, the internal soft shutdown transistor is activated, pulling down the VH node to bring the SiC FET gate-source voltage to minimum and turning off the SiC FET. Note that Soft Shutdown behaves the same in all DESAT shutdown conditions, not only in the shorted load condition discussed here. As seen in 5. Adjustable Soft Shutdown, if external BOM is added to adjust Soft Shutdown time to a lower value, the SiC FET may be turned off quickly enough to avoid damage. When considering adjustment of Soft Shutdown, one should consider that there is a tradeoff between the Soft Shutdown duration and the height of the VDS voltage spike. A faster shutdown results in a higher VDS spike, whereas a slower shutdown results in a lower VDS spike.

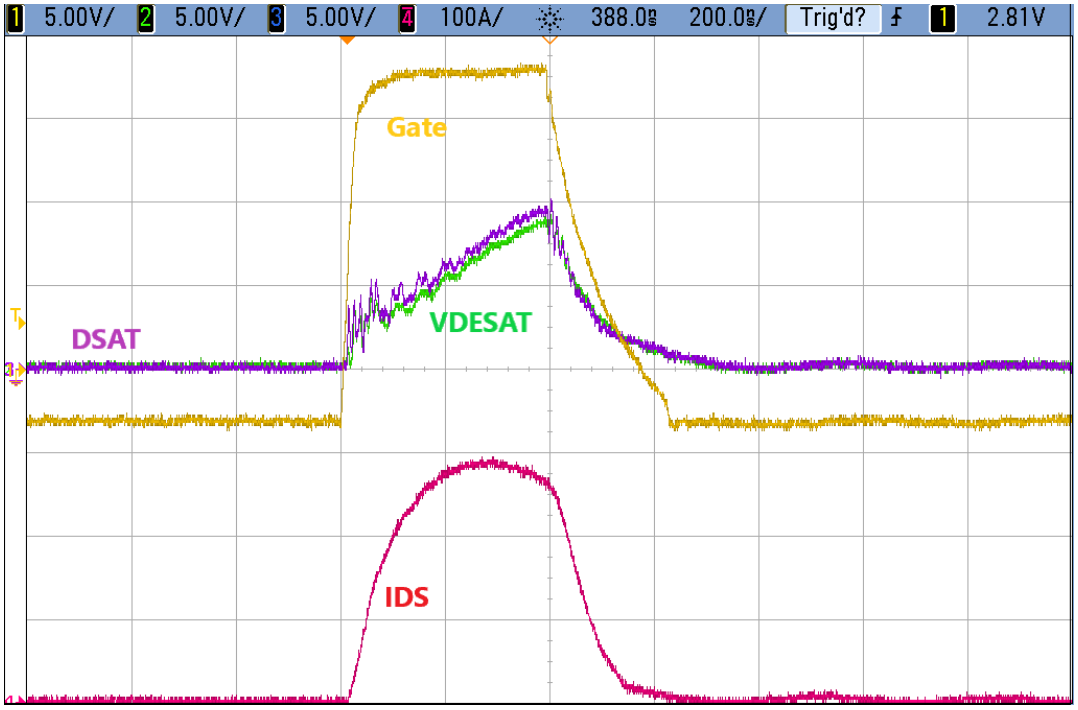

Figure 4.7. DESAT Protection Behavior in the Case of Shorted Load

5. Adjustable Soft Shutdown

IGBTs have slow switching speeds, and, as a result, can work with the standard Soft Shutdown time of a few µs designed into the Si828x. SiC devices, however, switch at much faster speeds, and reducing the Soft Shutdown time can help achieve reductions in overall DESAT protection response times. In order to provide adjustability to the Soft Shutdown feature, an external RSS and a PNP transistor, Q3, are added to the Si828x DESAT circuits. As shown in Figure 5.1 External BOM for Flexible Soft Shutdown (RSS = 30 Ohms) on page 16, the internal Soft Shutdown MOSFET resistor is 50 Ω, while the value of the external RSS can range from 0 Ω and greater. Q3's base is controlled by VH; the emitter is attached to the external RSS while the other end of the external RSS is attached to RH. A diode is inserted between VH and RH to allow the internal shutdown activity to proceed in a coordinated fashion with the external shutdown activity. See Figure 5.1 External BOM for Flexible Soft Shutdown (RSS = 30 Ohms) on page 16 for a depiction of how the enhanced adjustable soft shutdown circuit works.

5.1 External BOM for Flexible Soft Shutdown (RSS = 30 Ohms)

When VH rises, the internal DSAT pin current source Ich also is turned on to prepare for DESAT detection of a rise in S1 VDS due to an overcurrent fault. As the fault happens the DSAT pin voltage rises and crosses the DESAT threshold. This disables Dr-H and Dr-L and invokes the Soft Shutdown transistor action to pull down VH. As VH falls to a PNP VBE below Gate 1, the Gate 1 node will be pulled down toward -VSSB and S1 will be shut down. The current gain of Q3 allows an enhanced Soft Shutdown response which is limited by the value of RSS (external). RSS is the point of adjustability for Soft Shutdown.

Component values here are RH = RL = 0 Ω, RSS = 30 Ω (external), CBL = 270 pF (good noise immunity), and RI = 2.2 k Ω.

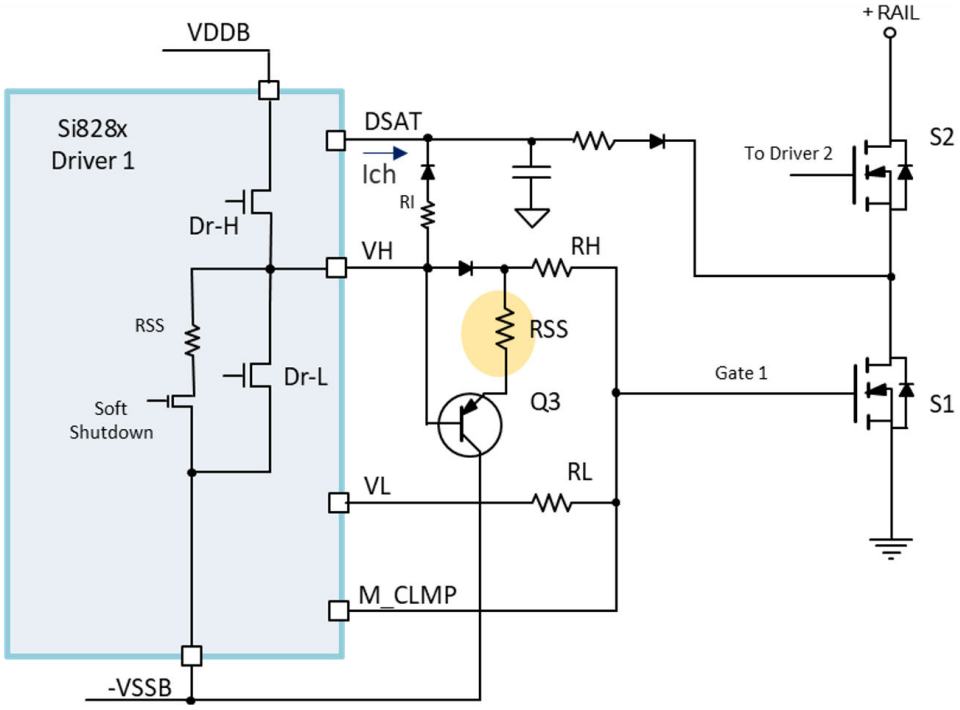

Figure 5.1. External BOM for Flexible Soft Shutdown (RSS = 30 Ohms)

The soft shutdown duration can be roughly estimated based on the RSS value and the SiC/IGBT total gate capacitance Cg:

$$tSSD = 3 \times RSS \times Cg$$

For example:

RSS = 30 Ohms

Cg = 9.1 nF (C3M0016120K)

$$tSSD = 3 \times 30 \times 9.1 \times 10^{-9} = 820ns$$

There is some inaccuracy in the above calculation due to the dynamic Miller capacitance value.

The figure below exhibits the same behaviors as seen prior to the addition of the external Q3 and RSS, but the addition of external elements allows for more flexible control of the device shutdown. In this case the shutdown time is shortened to 740 ns from the standard shutdown time of 1.3µs. The total shorted circuit response time is now 710 ns (zero current to zero current), Additionally note the VDS spike of 132 V is a bit higher due to faster di/dt of the initial drain current ramp down.

Notice that there are differences between the gate voltage shutdown time and the short-circuit response time. The gate voltage is the control signal. It causes the current to start and stop. But there is some phase difference between gate voltage and drain current due to the characteristic of the SiC. Note that the drain current drops more rapidly than the gate voltage and may go to 0 A before the gate voltage gets to 0 V.

The figure below shows Soft Shutdown behavior with an external RSS resistor value of 30 Ω, but the Soft Shutdown period can be reduced further by adjustment of the external RSS resistor. As seen in the next section, an even faster Soft Shutdown time results in a higher di/dt on the drain current and a higher voltage spike on S1's VDS, which may or may not be of concern in specific cases such as when switch devices with lower breakdown voltages are used.

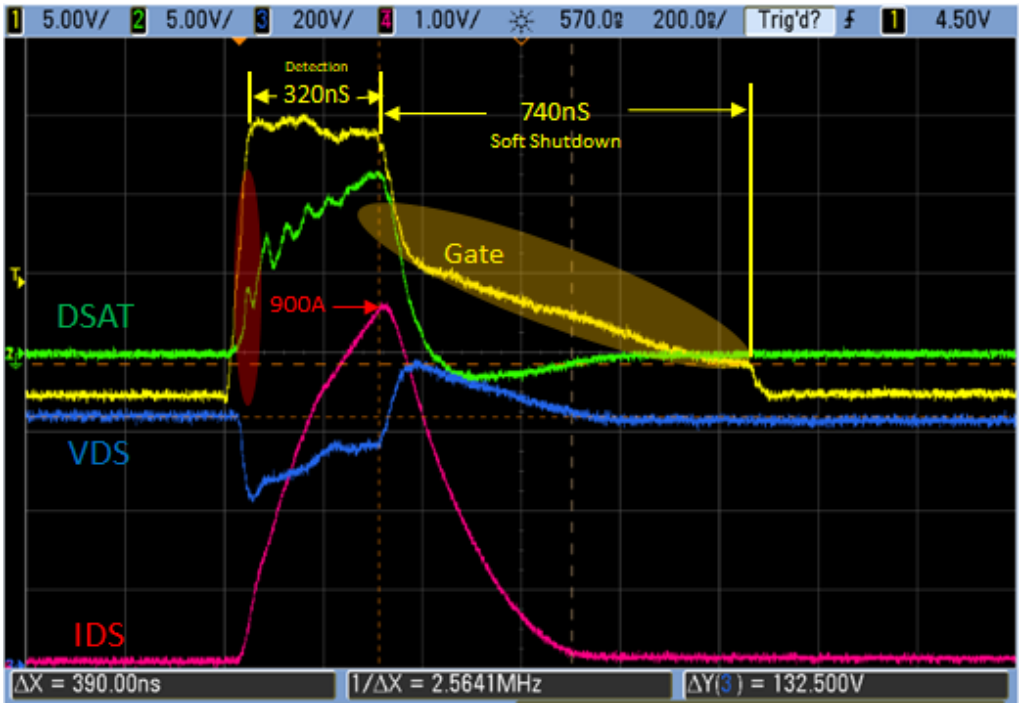

Figure 5.2. Signals for External BOM for Flexible Soft Shutdown (C3M0016120K)

5.2 External BOM for Flexible Soft Shutdown (RSS = 5 Ohms)

As noted, the Soft Shutdown period can be reduced further by adjustment of the external RSS resistor. The figure below shows an aggressive reduction of the period by adjusting the external RSS resistor to 5 Ω. With this adjustment, detection time remains at 320 ns, but the reduced RSS allows a stronger current to be applied to Gate 1 by Q3's emitter. This causes Gate 1 to be pulled down rapidly toward -VSSB, reducing the total short circuit response time to 500 ns and reducing Soft Shutdown time to 340 ns. The reduced short circuit response time results in the higher di/dt of the falling S1 drain current. This further results in a tradeoff seen in the increased VDS voltage spike of 268 V. When considering adjustment of Soft Shutdown, one should consider that there is a tradeoff between the Soft Shutdown duration and the height of the VDS voltage spike. A faster shutdown results in a higher VDS spike, whereas a slower shutdown results in a lower VDS spike.

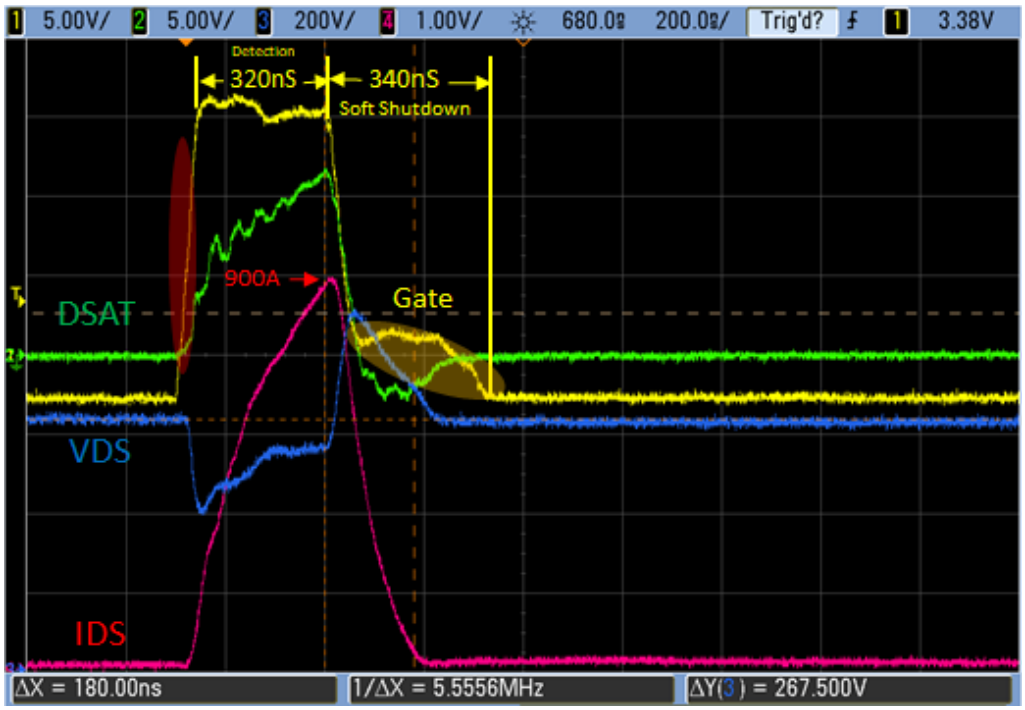

Figure 5.3. Signals for External BOM for Flexible Soft Shutdown (RSS = 5 Ohms, C3M0016120K)

6. External Miller Clamp: Q4

IGBT power circuits are commonly connected in a half bridge configuration with the collector of the bottom IGBT tied to the emitter of the top IGBT.

When the upper IGBT turns on (while the bottom IGBT is in the off state), the voltage on the collector of the bottom IGBT flies up several hundred volts quickly (fast dv/dt). This fast dv/dt induces a current across the IGBT collector-to-gate capacitor (C_{CG}) that constitutes a positive gate voltage spike which can turn on the bottom IGBT. This behavior is called Miller parasitic turn on and can be destructive to the switch since it causes shoot through current from the rail right across the two IGBTs to ground. The Si828x has an integrated Miller clamp device to protect against this phenomenon.

The Si828x Miller clamp's purpose is to clamp the gate of the SiC FET or IGBT device being driven by the Si828x to prevent IGBT turn on due to the collector C_{CG} coupling.

The Miller clamp device (Clamp) is engaged after the main driver had been on (VL) and has pulled IGBT gate voltage close to VSSB, such that one can consider the IGBT being already off. This timing prevents the Miller clamp from interfering with the driver's VL turned off operation. The engaging of the Miller Clamp is done by comparing the IGBT gate voltage with a 2.0 V reference (relative to VSSB) before turning on the Miller clamp's NMOS. Note that it is activated during driver low output duration and during DESAT fault ,when Vgate < 2 V.

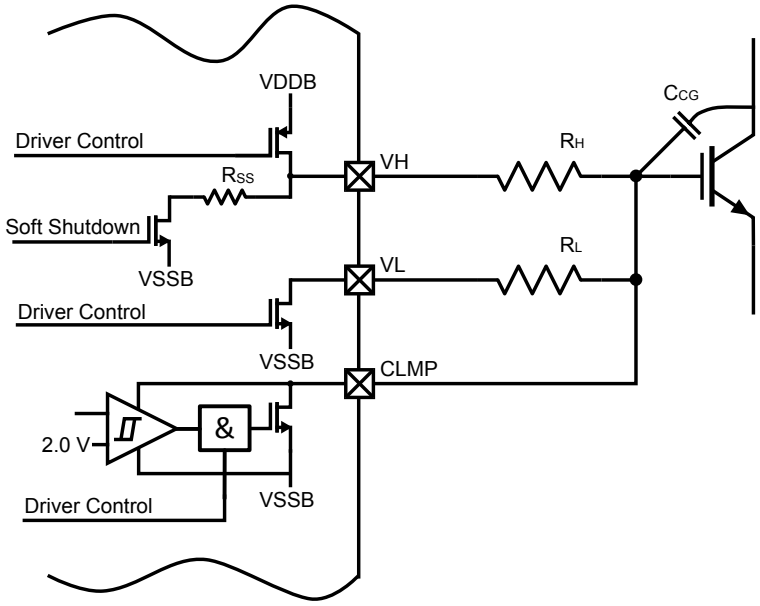

Figure 6.1. Miller Clamp Device

The figure below shows how the internal Miller clamp helps keep the low-side switch in the off state when the high-side switch turns on and its source rises very quickly. The clamp causes current to be extracted from the Drain-Gate capacitance through the gate node, such that this current does not cause a rise in the low-side switch VGS, and in fact assists this device in turning off.

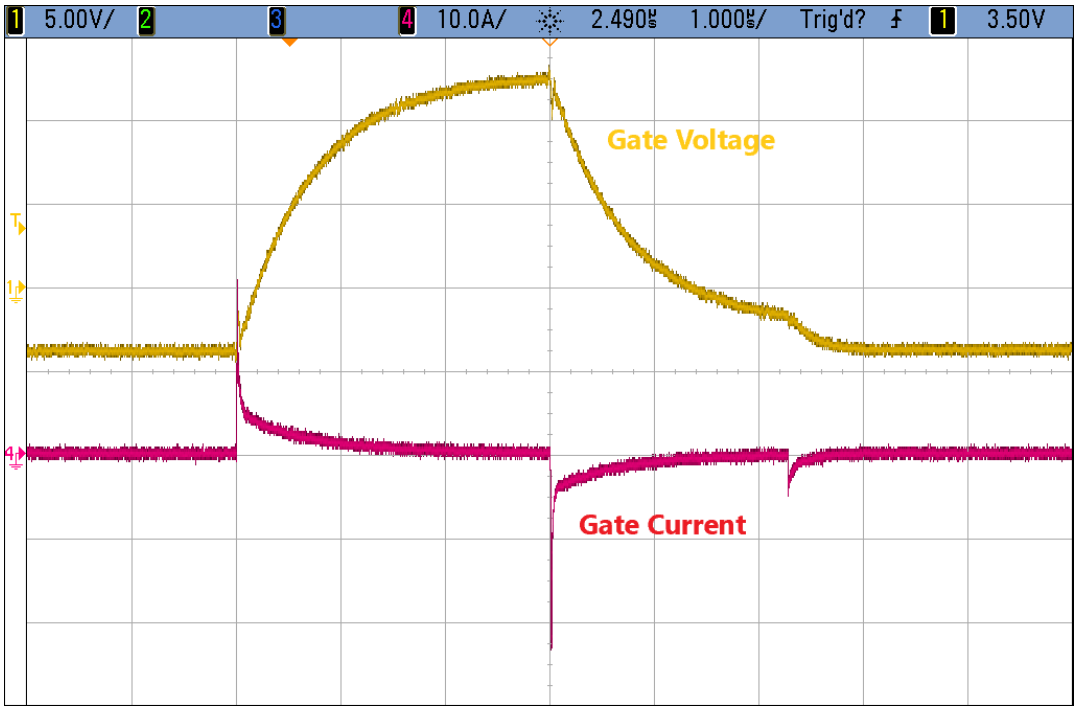

Figure 6.2. Internal Miller Clamp Behavior

Shown below in a SiC FET driver scenario, the circuit enhancement contains Q4/D5, a low-output-impedance follower circuit that is placed strategically between the SiC Gate and –VSSB to provide a low impedance connection to minimize Miller voltage spikes which could lead to false turn ons.

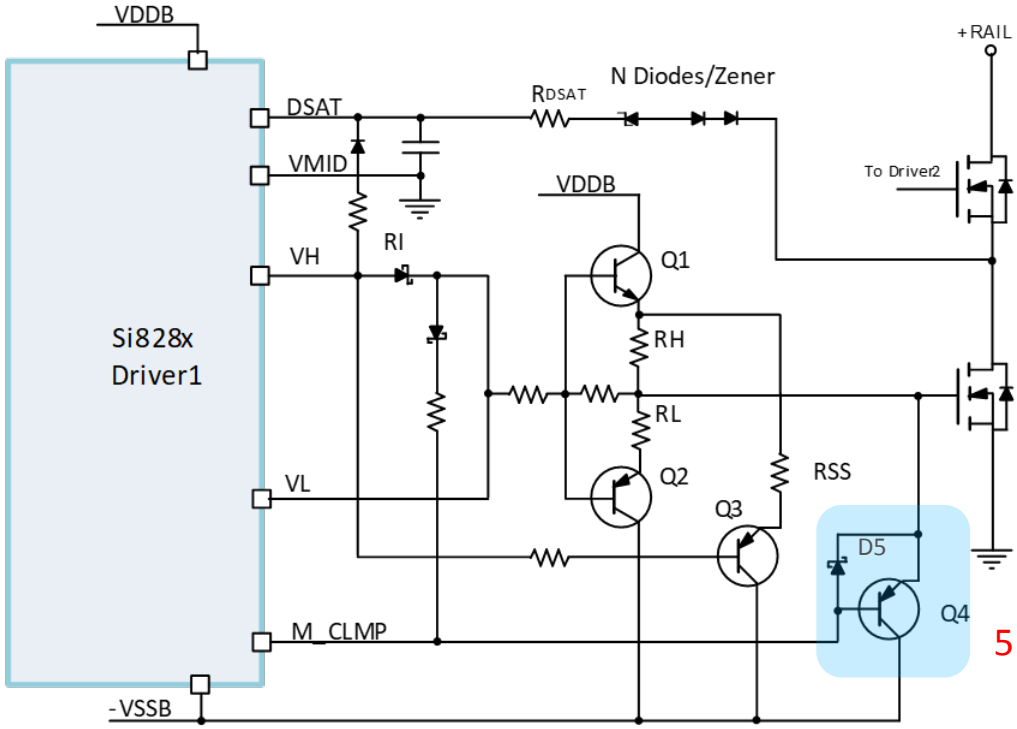

Figure 6.3. External Miller Clamp

The figure below shows how the external Miller clamp device improves Miller clamp behavior. As shown, the negative current pulse out of the gate is greater than that produced by the internal Miller clamp device. This will result in a more secure off state for the low-side switch when the high-side switch source rises rapidly during high-side switch turn on. The extra delay of the clamp action is due to the diode voltage drop of the external Miller clamp diode (D5). This diode drop causes the Miller clamp to turn on at reduced gate voltage 2 V to 1.3 V.

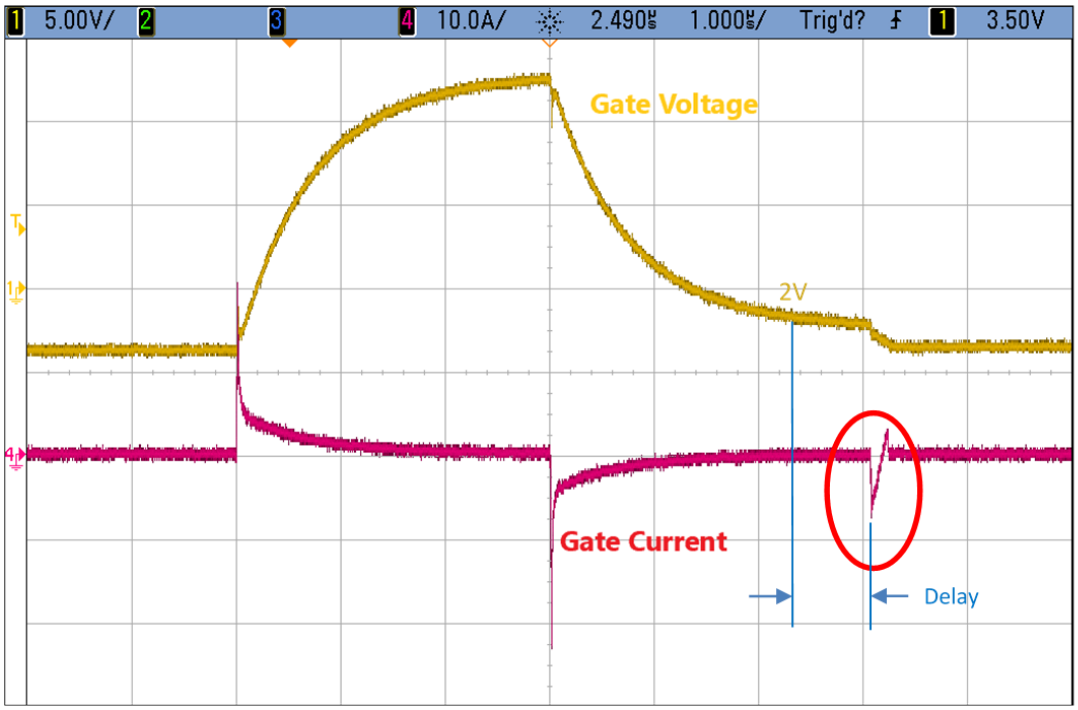

Figure 6.4. External Miller Clamp Behavior

7. Summary of All External Enhancements of the Si828x IsoDriver

The figure below shows all the external driver enhancement circuits for the Si828x family, including

1. Current Booster: Q1 and Q2
2. DESAT detection speed up circuit: RI, DI
3. DESAT threshold adjustment: RDSAT, RZ
4. Adjustable soft shutdown: Q3, RSS
5. External Miller clamp: Q4

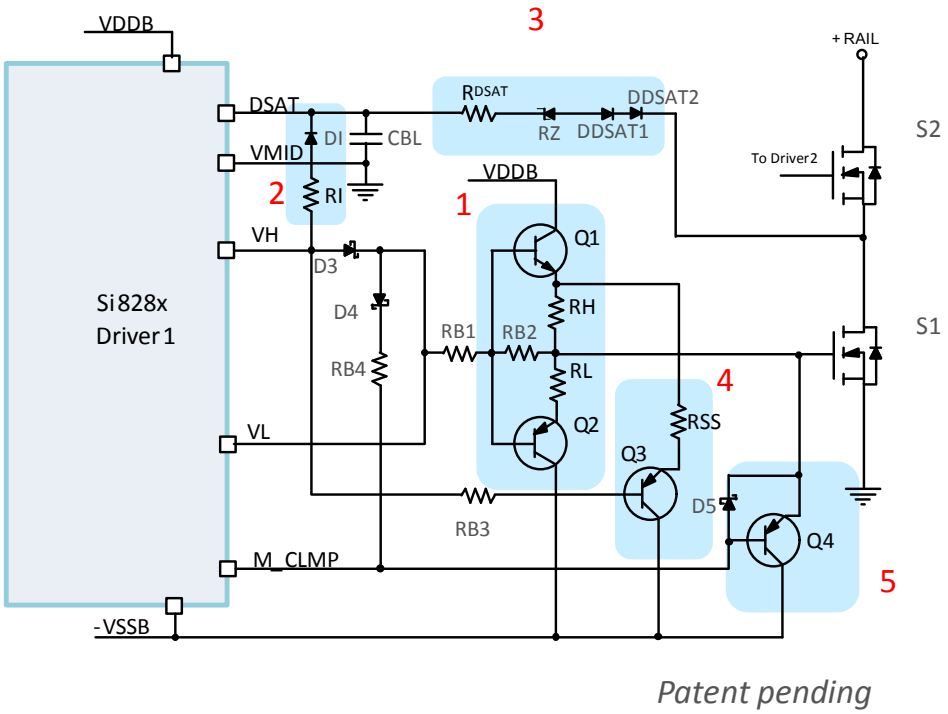

Figure 7.1. Total Gate Driver Enhancement Circuits

The following tables summarize the performance improvements made by external gate driver enhancements of the Si828x device.

Table 7.1. Performance Improvements

Improvement	Standard Response	Enhanced Response	Comment
Gate Drive Current	+3A, –6A	+20A, –30A	RH = RL = 0, Q1: FZT951, Q2: ZXTN2010
DESAT Detection Time	3.0 µs	320 ns	RI = 2.2 kΩ, Diode
DESAT Threshold	7 V	3.7 V	VZener = 3.3V
Device Shutdown Time	0.5 µs	340 ns	Q3, RSS = 5 Ω
Total Response Time	3.5 µs	660 ns	RI = 2.2 kΩ, Diode, Q3, RSS = 5 Ω
Miller Clamp Action	Suppression of Miller voltage spike	Improved suppression of Miller voltage spike	Q4 PNP, D5

Table 7.2. Booster Pair (Q1, Q2) Recommendations

NPNQ1	PNP Q2	Performance	Package
FZT951	ZXTN19060CG	(+20 A / –30 A)	SOT223
PHPT60415NY	PHPT60415PY	(+14 A / –14 A)	SOT669 (LFPAK56)
PHPT60410PY	PHPT60410NY		SOT669 (LFPAK56)
PHPT60606PY	PHPT60606NY		SOT669 (LFPAK56)
MJD45H11	MJD44H11		DPAK
ZXTN2010ZTA	ZXTP2012ZTA	(+20 A / –30 A)	SOT89

Table 7.3. Other Transistor (Q3, Q4) Recommendations

PNP Q3	PNP Q4
MMBT2907	Same as Q2 from Table 7.2 above, paired with appropriate Q1.

Table 7.4. Remaining Component Recommendations

Ref Des	Part Number	Vendor	Package	Description
CBL	C0603C0G500-391K	Venkel	0603	CAP, 390 pF, 50 V, ±10%, C0G, 0603
DDSAT1	1N4148W	Diodes Inc.	SOD-123	DIO, FAST, 100 V, 2 A, SOD123
DDSAT2	1N4148W	Diodes Inc.	SOD-123	DIO, FAST, 100 V, 2 A, SOD123
DZ1	MMSZ4686T1G	On Semi	SOD-123	DIO, ZENER, 3.9 V, 500 mW, SOD123
DI	1N4148W	Diodes Inc.	SOD-123	DIO, FAST, 100 V, 2 A, SOD123
D3	RB160MM-30TF	Rohm Semiconductors	SOD-123	DIO, SCHOTTKY, 30 V, 1 A, SOD123
D4	1N4148W	Diodes Inc.	SOD-123	DIO, FAST, 100V, 2 A, SOD123
D5	1N4148W	Diodes Inc.	SOD-123	DIO, FAST, 100V, 2 A, SOD123
RDSAT[1]	RC0603FR-072K2L	Yageo	0603	RES, 2.2K, 1/10 W, ±1%, Moisture Resistant, ThickFilm, 0603
RB1	CR1206-4W-10R0F	Venkel	1206	RES, 10 Ohm, 1/4 W, ±1%, ThickFilm, 1206
RB2	CR1206-4W-20R0F	Venkel	1206	RES, 20 Ohm, 1/4 W, ±1%, ThickFilm, 1206
RH[1]	CRCW20103R00FKEFHP	Vishay	2010	RES, 3.0 Ohm, 1 W, ±1%, ThickFilm, 2010

Ref Des	Part Number	Vendor	Package	Description
RL[1]	CRCW20103R00FKEFHP	Vishay	2010	RES, 3.0 Ohm, 1 W, ±1%, ThickFilm, 2010
RI[2]	RC0603FR-072K2L	Yageo	0603	RES, 2.2K, 1/10 W, ±1%, Moisture Resistant, ThickFilm, 0603
RSS[1, 3]	CR1206-4W-12R0FT	Venkel	1206	RES, 12 Ohm, 1/4 W, ±1%, ThickFilm, 1206

Note:

1. This component value may be adjusted to adapt to specific design requirements.
2. RI has a recommended value of 2.2 kΩ but is adjustable according to Equation 4.1.
3. RSS has a recommended value of 12 Ω but may be adjusted to set Soft Shutdown duration.

7.1 Protection Components

Due to the parasitic inductance in the layout, voltage spikes are generated during high current switching. It is prudent to add the following component to protect the gate driver:

- Power pin protection: 22 V Zener diode from VSSB (anode) to VDDB (cathode). Suggested: Diodes Inc SMAZ22-13-F
- Gate protection: diode from VSSB (anode) to gate (cathode), diode from gate (anode) to VDDB (cathode). Suggested: On Semi MBR1H100SF
- DSAT pin protection: Zener diode from VSSB (anode) to DSAT pin (cathode). Suggested: On Semi MMSZ4702T1G

8. Conclusion

This application note has discussed Si828x gate drive circuit enhancements and their associated performance improvements, including a current drive booster which will increase gate current drive above 20 A, circuitry for reducing DESAT protection response time below 1µs, a DESAT threshold adjustment which allows a threshold below the nominal 7 V, a method of adjusting the soft shutdown time to meet application needs, and an external enhancement of the internal Miller clamp, improving capture of the Miller clamp current spike which occurs when an external high-side transistor is turned on. These enhancements not only improve performance when driving IGBTs, they provide excellent performance when driving SiC FET devices as well. It is important to note that each of these enhancements may be implemented individually or in combination.

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