Crossing a New Frontier of Multiband Receivers with Gigasample ADCs—Part One

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Introduction

The analog-to-digital converter (ADC) has been a staple of communications receiver design for quite some time now. As communications technology continues to evolve, consumers are demanding faster data rates and cheaper services. Backhaul service providers who enable this technology are confronted with a dichotomous situation. Faster data rates mean more bandwidth, which translates to faster data converters that convert the analog air waves to be digitally processed. However, faster data converters (GSPS or gigasample per second converters)—widely known as RF sampling ADCs—also produce huge amounts of data that have to be processed at a much higher speed in these DSP chips. This invariably increases the cost of operating a radio receiver.

The solution lies in clever design of the silicon that forms the RF sampling ADC. Taking advantage of the silicon processing advancements (thank you, Moore's law), RF sampling ADCs mix in custom digital processing blocks that are more power and area efficient compared to existing FPGAs. The use of these digital signal processing blocks also results in lower data rates, which enable the use of lower cost FPGAs. This is a win-win situation for operators since they can sample at high frequencies using these GSPS ADCS, use the internal digital downconverters (DDCs) to process the data at speed, and send it out at a manageable (low) data rate to a cheaper FPGA (or existing generation ASIC) for further baseband processing.

The other advantage of using RF sampling ADCs with the DDCs is that this enables a more flexible, compact, cost-effective way to implement a dual-band radio system. Dual-band radio systems have been around for years now. Base station systems designers have traditionally implemented the dual-band radio systems by making use of two separate radio paths, one for each band. This article discusses a method to utilize a multiband radio receiver using an RF sampling ADC like the AD9680 to digitize and process two separate widely used bands. Part One of the article explains a block diagram level implementation and discusses advantages of using a GSPS ADC for a dual-band radio system. Part Two of the article will discuss an implementation and data analysis of TDD LTE bands 34 and 39 (also known as band A and band F, respectively) with data analysis to show converter performance.

Traditional Dual-Band Radio Receiver

In order to cater to customer demands for dual-band radios and meet overall system-level performance, base station designers resorted to what they knew best: Replicate a radio's design twice and tune one for each band. This meant that the designer had to have two separate radio hardware designs tuned to the two bands that the customer had chosen.

For example, if there was a need to build a radio receiver that could support TDD LTE band 34 (band A: 2010 MHz to 2025 MHz) and band 39 (band F: 1880 MHz to 1920 MHz)[1], the designer would pack two radio receiver designs. The frequency plan for the TDD LTE bands is shown in Figure 1.

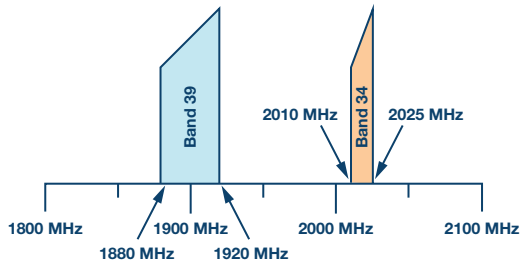

Figure 1. Frequency plan showing TDD LTE bands 34 and 39.

The traditional approach to designing a dual-band radio receiver to accommodate these bands would be to implement two separate receiver chains, one for each band. A block diagram representation of the dual-band radio receiver is shown in Figure 2 below.[2]

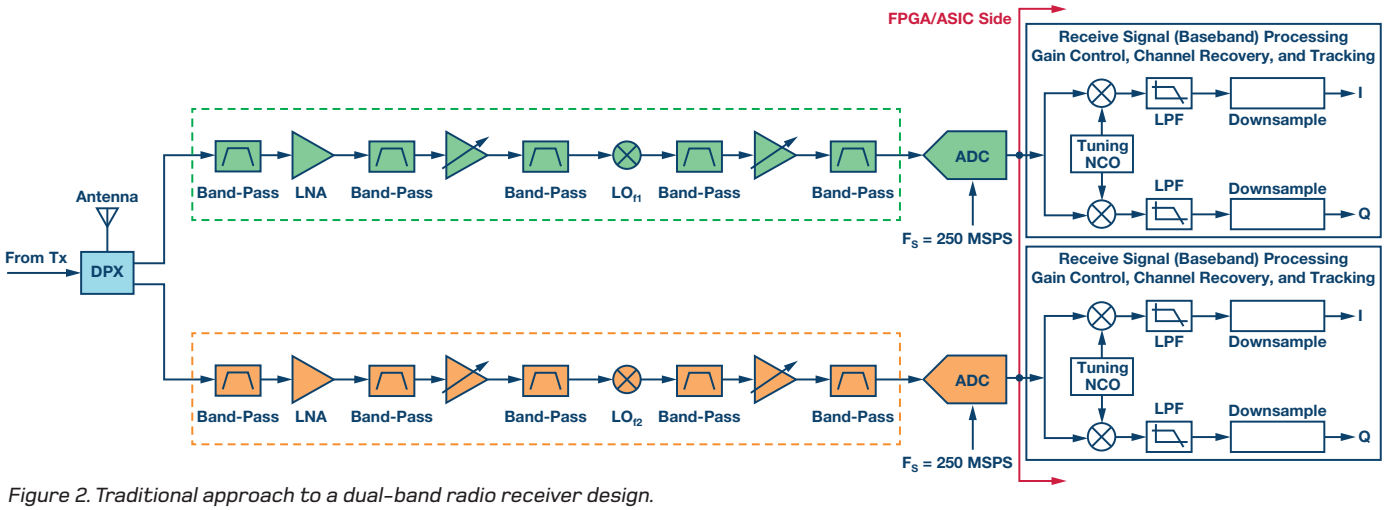

Figure 2. Traditional approach to a dual-band radio receiver design.

Figure 2 shows a traditional implementation of a dual-band radio. This implementation is fairly expensive to implement because it practically is two radio receivers in one system. Every processing element is duplicated in order to accommodate the respective bands. This also applies to FPGA resources. Every processing element is duplicated in order to accommodate the respective bands resulting in duplication of FPGA resources, increased system cost and complexity, and additional power. In terms of the interface to the FPGA, the FPGA resources will have to be doubled to accommodate the two ADC data streams. Figure 3 shows a block diagram representation of the FPGA I/O resource requirements or a dual-band radio receiver system design. It shows both an LVDS and a JESD204B ADC interface. The LVDS data rates are lower, but the FPGA will need a higher I/O count. The JESD204B interface requires a lesser number of I/O resources from the FPGA, but the lane rates can be higher, which could warrant a more expensive FPGA.

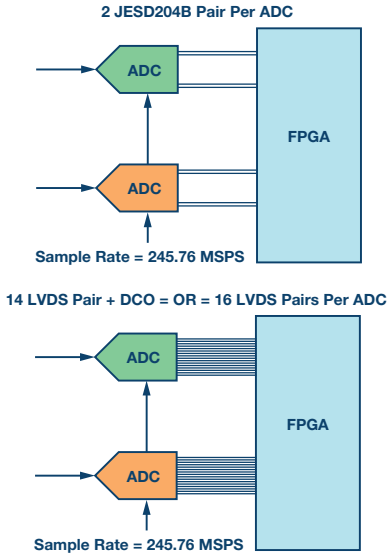

Figure 3. FPGA interface requirements for a traditional approach to a dual-band radio receiver.

Dual-Band Radio Receiver Using RF Sampling (GSPS) ADCs

The RF sampling or GSPS ADC can offer system design flexibility. By taking advantage of the deep submicron process technology, the GSPS ADCs can pack digital processing blocks that can manipulate the data at speed with much less power consumption compared to an FPGA. At the heart of the RF sampling ADC is a high bandwidth analog sampling core that samples at GHz speeds. Following the analog core is a plethora of digital signal processing elements. These digital downconverters can be used to extract the respective bands. A block diagram of the internals of an RF sampling ADC setup for a dual-band receiver is shown in Figure 4. The DDCs, in addition to processing the signals, also reduce the lane rate of the data on the JESD204B lanes.

With the added digital signal processing blocks, the GSPS ADC can now single-handedly accommodate two bands for processing. This is a win-win situation for operators since they can sample at high frequencies using these RF Sampling ADCS, use the internal digital downconverters (DDCs) to process the data at speed, and send it out at a manageable (low) data rate to a cheaper FPGA (or existing generation ASIC) for further baseband processing. The high bandwidth front end offered by these ADCs enables the system designer to capture a wide swath of frequencies (two radio bands, for example) and digitize it for signal processing. Figure 5 below shows a dual-band receiver system using a RF sampling ADC and internal DDCs to extract the bands. As is evident by comparing with the implementation in Figure 2, the dual-band receiver using the RF sampling ADC is significantly simpler in implementation. In this implementation the RF is mixed down to a high IF that is many hundreds of MHz wide, as opposed to many tens of MHz wide in the traditional dual-band approach. The BPF and VGA stage is optional and is dependent on what level of system performance is expected.

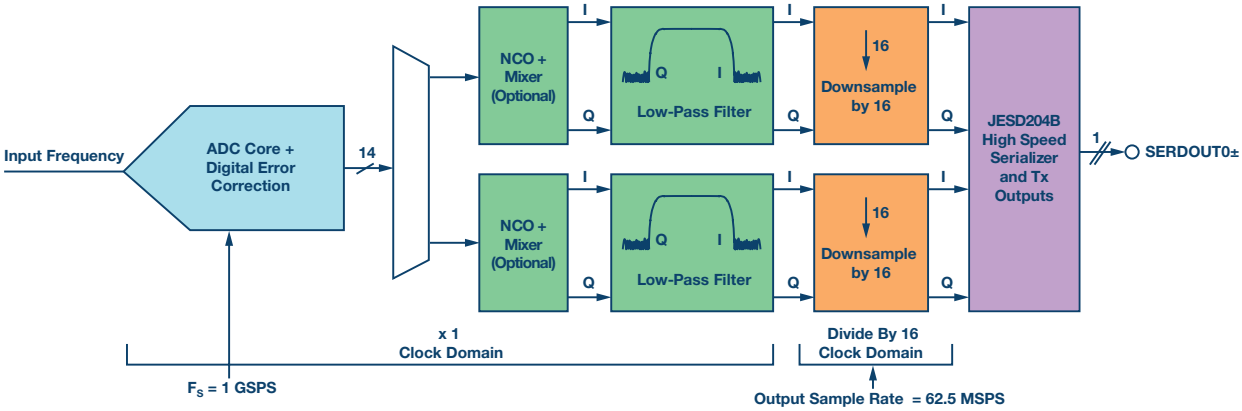

Figure 4. Block diagram representation of the RF sampling ADC showing the internal DDCs.

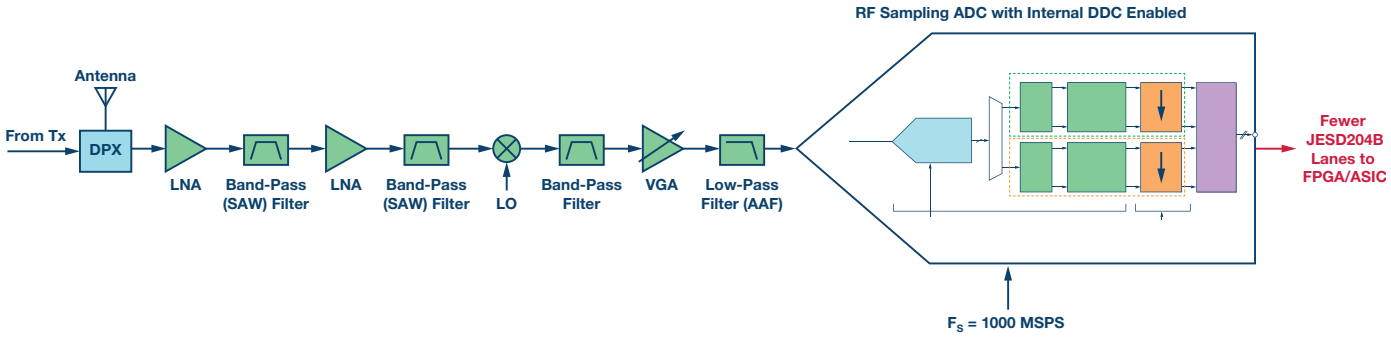

Figure 5. A dual-band radio receiver using the RF sampling ADC and internal DDCs to extract the bands.

Some of the advantages of using an RF sampling ADC for a dual-band radio system are explained below:

Simpler Front-End Design

A dual-band radio system design using a RF sampling ADC greatly simplifies the front-end network. For starters, there is only a need for a single front-end design instead of two (one for each band). This heavily reduces the bill of material for the system board. Then there is the AAF (antialiasing filter) requirement, which is a band-pass filter (BPF) for the two IF converter case, compared with a low-pass filter (LPF) for the GSPS ADC case. This is because the GSPS ADC oversamples the input signal.[3, 4] Now that the data is oversampled, the digital downconverters can do their job of decimating and filtering. If the frequency plan is such that the second- and third-harmonics fall out of band, this eases the requirements on the AAF.

Lower System Power, Smaller Form Factor

Instead of two LNAs, two mixers, and two IF ADCs as shown in Figure 2, there is only a need for one front end in the RF sampling case (Figure 5). This results in major power savings from a system-level power consideration. The lower system power clubbed with the need for a simpler front-end design allows systems to be made in smaller form factor.

More Efficient FPGA Utilization

When using an RF sampling ADC to implement a dual-band radio system, the DDCs are employed to extract the individual bands. Since DDCs decimate the data, the output sample rate is reduced. This results in many flexible configurations for the JESD204B interface. For example, if a dual ADC is sampling at 1 GSPS and is in full bandwidth mode, the line rate is calculated at 10 Gbps/lane over four lanes. The line rate for JESD204B converters from Analog Devices can be calculated as follows:

$$Lane\ Line\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times F_{OUT}}{L}$$ where,

M = number of converters (in this example, 2)

N' = number of converter bits per sample (in this example, 16)

10/8 = 8B10B overhead

F_{OUT} = output sample rate (Fsample/Decimation_Ratio; in this example, Decimation_Ratio = 1 for full bandwidth)

L = number of JESD204B lanes (in this example, 4)

If the same dual ADC is utilizing a total of four DDCs in a decimate-by-8 configuration, for example, then there are many configurations that the ADC will support, based on the number of lanes. The output sample rate becomes 125 MSPS (1 GSPS ÷ 8). The different configurations are listed in Table 1:

Table 1

DDC Configuration	M	L	Line Rate (Gbps/Lane)
Real	4	1	10
Real	4	2	5
Complex	8	2	10
Complex	8	4	5

These flexible configurations provide the systems designer the freedom to either use an expensive FPGA with higher line rate but better I/O lane density usage, or use an existing FPGA/ASIC that has line rate limitations.

Conclusion

The advent of the GSPS ADC in deep submicron silicon processes has ushered in a new era of radio architecture discussion and design. The GSPS ADC with its high bandwidth sampling core and the digital downconverter options offer a flexible pathway to rethink and redefine the radio architecture that will cater to the growing demands of the consumer. The reduction in power and space offered by these GSPS ADCs will lower the cost of ownership for these radio boxes. The flexible output options provided by the current generation ADCs with the JESD204B interface do not lock the systems designer into using an expensive high line rate FPGA or digital logic.

Part 2 of this article will discuss a use case involving TDD LTE bands 34 and 39 and its analyses in a multiband radio receiver using the AD9680.[5]

References

[1] E-UTRA Bands.

[2] Walt Kester. *The Data Conversion Handbook*. Analog Devices, Inc, 2005.

[3] Umesh Jayamohan. "Not Your Grandfather's ADC: RF Sampling ADCs Offer Advantages in Systems Design." Analog Devices, Inc, 2015.

[4] Oversampling.

[5] AD9680. Analog Devices, Inc.

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