Improving Precision Data Acquisition Signal Chain Density Using SiP Technology

By **Ryan Curran**

Share on

A common desire in the precision data acquisition market space is to improve the density of the signal chain while maintaining performance. As more applications are moving to an ADC-per-channel approach, or trying to fit more channels into the same form factor, channel density is a great concern for many data acquisition signal chain designers. On top of this, there has been a trend to make precision circuitry easier to use and more easily achieve data sheet performance. This provides an opportunity to build subsystems that address these concerns by implementing signal chains using system-in-package (SiP) technology.

The first family of devices produced by Analog Devices as a result of this subsystem strategy is the new ADAQ798x data acquisition products. The ADAQ798x is a 16-bit analog-to-digital converter subsystem that integrates four common signal processing and conditioning blocks into a SiP design that supports a variety of applications. The device also contains the most critical passive components, eliminating many of the design challenges associated with traditional signal chains that utilize successive approximation register (SAR) analog-to-digital converters (ADCs). These passive components are crucial to achieving the specified device performance.

When looking across applications and markets that utilize SAR ADCs, such as industrial, instrumentation, communications, and healthcare, it was seen that certain sections of data acquisition signal chains are very common across these applications, while some portions of the signal chains can differ extensively. It was seen that these signal chains use a varying array of input sources and sensors. As a result, there are going to be various forms of signal conditioning implemented before presenting the signal to the ADC. With the sources varying, this means the system full scales can be different and require different reference values to maximize dynamic range. Some applications are multichannel and, therefore, implement a front-end multiplexer. Differing supply schemes would be implemented based upon the key performance criteria of the application. However, regardless of the application, there are components that are common to many of these applications. The ADAQ7980 and ADAQ7988 are part of an all Analog Devices active component solution that contains a high accuracy, low power, 16-bit SAR ADC; a low power, high bandwidth, high input impedance ADC driver; a low power, stable reference buffer; and an efficient power management block. These signal chain components have been integrated into a data acquisition subsystem using SiP technology.

Housed within a small footprint 5 mm × 4 mm LGA package, this new style component will simplify the design process for data acquisition systems. The ADAQ798x's level of system integration solves many design challenges, yet the device still provides the flexibility of a configurable ADC driver block to allow for gain and/or common-mode adjustments. A set of four device supplies provides optimal system performance, but single supply operation is possible with minimal impact on the device's operating specifications. The ADAQ798x family provides a significant level of integration while still being flexible enough to adapt to a wide assortment of applications.

When developing this product, ADI analyzed common design mistakes to determine how to help solve these challenges. It was seen that many of these signal chain level design mistakes were primarily centered around two areas of the SAR ADC—the reference input and the analog input. Many of these signal chain errors are associated with the circuitry peripheral to the ADC that is critical to the overall analog-to-digital conversion performance. With respect to the reference, common mistakes include improper layout and sizing of the reference bypass capacitor, insufficient drive strength of the reference source, and too large of a noise spectral density generated by the reference source. These unsuitable design conditions at the reference input of a SAR ADC can lead to the ADC making incorrect bit decisions. As for the ADC analog input, common design issues that have been observed include incorrect ADC driver selection, incorrect filter bandwidth between the ADC driver and the ADC, and incorrect filter capacitor dielectric material choices. Any combination of these system-level design issues can lead to severe degradation of ADC conversion performance. The choices made in developing the ADAQ798x devices were intended to address these concerns.

As just discussed, to achieve data sheet performance from a SAR ADC-based conversion system, there are some design considerations that must be taken into account. The SAR ADC reference source and analog input source characteristics are critical to successfully designing the conversion signal chain. Typically, a SAR ADC requires a low impedance reference source and a large, properly laid out decoupling capacitor. This bypass capacitor is used to replenish charge consumed by the ADC during the SAR bit trials and can be thought of as a component of the SAR array that is external to the ADC. The ADC also needs an analog input source with sufficient noise performance and bandwidth to properly settle the ADC input to the desired resolution. Figure 1 shows the block diagram of the ADAQ798x devices.

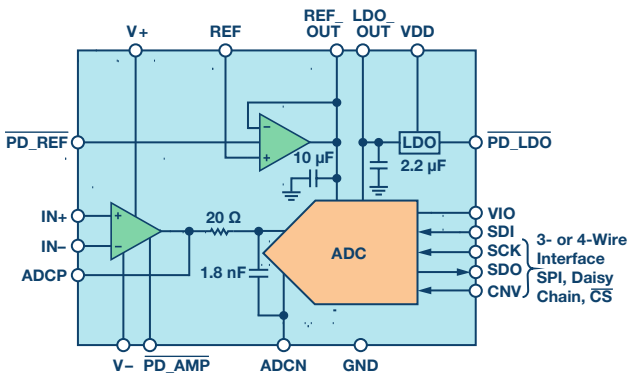

Figure 1. ADAQ798x block diagram.

As seen in Figure 1, ADAQ798x houses a reference buffer and a corresponding 10 µF decoupling capacitor. The decoupling capacitor is ideally laid out in proximity to the reference input of the ADC. The goal of this component placement is to reduce all parasitic impedances between the decoupling capacitor and the SAR capacitor array. This path should be as low of an impedance as possible to allow the capacitor to quickly add charge onto the SAR array to be redistributed as part of the conversion process. As well, the trace resistance between the reference buffer and the decoupling capacitor has been controlled. A trace dimension was chosen to provide a resistance that will keep the reference buffer stable, while not causing a voltage drop large enough to create a conversion gain error. The amplifier used to buffer the reference signal is configured in unity gain. This presents a high impedance input to the external reference source instead of presenting the traditional switched capacitor load of the SAR ADC reference input. The ADAQ798x user can now implement a lower power or unbuffered reference to drive the ADAQ798x reference input (REFIN) pin. By presenting a high impedance, this also gives the user more flexibility in choosing the physical PCB location of the reference source. By using this SiP component, the reference source layout has become much less critical because of the inclusion of a well controlled reference buffer within the ADAQ798x. By only including a buffer and not the reference source itself, the user has the freedom to choose a wide range of reference values and ultimately maximize the system dynamic range with this reference selection because the reference sets the converter full-scale voltage.

The ADAQ798x also features an ADC driver and corresponding low-pass filter between the driver and the ADC input. The filter bandwidth selection is critical to achieving desired performance levels. The bandwidth is selected as a trade-off between settling time and filtering wideband noise from the high speed ADC driver. Any disturbances at the ADC input node must be settled to a sufficient resolution within the acquisition time of the ADC. When a SAR ADC is performing its conversion process, the ADC input is disconnected from its external input sources. During the conversion, the voltage potential at the ADC input could change. However, at the end of conversion, the voltage on the SAR capacitor array is essentially the same as it was when the conversion started. When the ADC returns to acquisition (track) mode, the SAR capacitor array load is now present at the ADC input. This capacitance is placed in parallel with the capacitor from the external low-pass filter. With differing voltages on these capacitors, a charge redistribution will occur to balance out the voltage on all of these capacitors. This will result in a voltage step at the ADC input that needs to be settled during the acquisition period. The worst-case step occurs when a full-scale transition is presented to the ADC. This scenario can arise in systems with a multiplexed input. This voltage step is attenuated by the ratio of the external capacitor and the internal SAR capacitance. The ADAQ798x products feature a low-pass filter capacitor of 1800 pF. Assuming a 5 V reference voltage, the maximum ADC input voltage step is calculated as follows:

$$V_{STEP} = \frac{5\text{ V} \times C_{SAR}}{C_{EXT} + C_{SAR}} = \frac{5\text{ V} \times 27\text{ pF}}{1800\text{ pF} + 27\text{ pF}} = 73.9\text{ mV}$$

This voltage step must be settled within the minimum acquisition time of 290 ns. The number of time constants required to settle this voltage step can be calculated as the natural logarithm of the ratio of the step size to the settling error. The settling error is chosen to be ½ LSB. Therefore, the number of time constants is found by:

$$\#\ of\ Time\ Constants = \ln\left(\frac{V_{STEP}}{V_{half\_LSB}}\right) = \ln\left(\frac{73.9\text{ mV}}{\frac{5\text{ V}}{2^{16+1}}}\right) = 7.57$$

With the number of time constants known, then the tau (τ) of the RC low-pass filter can be determined:

$$\tau = \frac{Minimum\ Acquisition\ Time}{\#\ of\ Time\ Constants} = \frac{290\text{ ns}}{7.57} = 38.3\text{ ns}$$

This tau can be used to determine the required filter bandwidth with the following equation:

$$RC\ Bandwidth = \frac{1}{2 \times \pi \times \tau} = \frac{1}{2 \times \pi \times 38.3\text{ ns}} = 4.15\text{ MHz}$$

To provide some margin and utilize standard value components, the ADAQ798x products feature a filter composed of a 20 Ω resistor and 1800 pF capacitor. This provides a filter bandwidth of 4.42 MHz, thus allowing the ADAQ798x filter to settle the largest anticipated voltage steps within the acquisition time of the ADC. The filter bandwidth calculated also represents the trade-off point between noise filtering and settling. Using a filter bandwidth near the minimum needed to ensure settling will maximize the noise filtering benefit of the passive low-pass filter.

While the voltage step from the SAR ADC returning to acquisition mode is the limiting factor in the filter settling calculation, it should be noted that the filter can also settle the actual voltage change from a multiplexer full-scale step well within the minimum conversion period of 1 µs. To settle a full-scale step to a ½ LSB resolution requires 11.78 time constants. This is calculated from the natural logarithm of N+1 number of quantization levels. In this case, 2^{17} or 131072 codes. 11.78 time constants at 38.3 ns per time constant is approximately 450 ns, which is of no concern as compared to the 1 µs conversion period. This assumes the multiplexer channel is switched directly after a conversion is initiated.

The ADC driver bandwidth is also extremely important to ensure proper performance of the conversion signal chain. In unity gain, the limiting factor in settling is the voltage step that needs to be settled in 290 ns that is associated with the converter returning to acquisition mode. Therefore, in this case, the small signal bandwidth is the most important amplifier bandwidth specification. To settle a multiplexer full-scale step within the minimum conversion period of 1 µs, an ADC driver large signal bandwidth must be maintained that allows for 11.78 time constants in the 1 µs time period.

The ADC driver should not contribute excessive noise to the conversion signal chain. The total subsystem noise performance is calculated as the root-sum-square combination of the ADC noise, the ADC driver noise, and the reference buffer noise. Due to the limited bandwidth of the reference circuit as a result of the large bypass capacitor, the reference buffer noise is negligible in the RSS calculation. A target for the ADC driver noise in a unity gain configuration has been chosen to be no greater than ⅓ of the ADC noise. The ADC driver is specified to have a noise spectral density of 5.2 nV/√Hz. To calculate the overall system noise, the ADC driver's noise spectral density must be converted to µV rms with the following equation:

$$v_{n,rms} = \frac{Noise}{Gain} \times e_{n,rms} \times \sqrt{\frac{\pi}{2} \times RC\ Filter\ Bandwidth} = (1) \times \frac{5.2\text{ nV}}{\sqrt{\text{Hz}}} \times \sqrt{\frac{\pi}{2} \times 4.42\text{ MHz}}$$

$$v_{n,rms} = 13.7\ \mu\text{V rms}$$

The ADC features a typical dynamic range specification of 92 dB with a 5 V reference. The noise floor of the ADC can be calculated as follows:

$$ADC\ Noise\ Floor = V_{full\text{-}scale,rms} \times 10^{-DR/20} = \frac{5}{2\sqrt{2}} \times 10^{-92/20} = 44.4\ \mu\text{V rms}$$

With an ADC driver noise floor of 13.7 µV rms, this falls below the target of ⅓ of the ADC noise. The overall system dynamic range is reduced from 92 db to 91.6 dB due to the noise contribution of the ADC driver in a unity-gain configuration. Because of the ADC driver's limited impact on system noise, there is no need to change the low-pass filter bandwidth for lower sample rate applications that provide more settling time due to longer acquisition periods. The best improvement in unity gain one could hope for by reducing the filter bandwidth would be gaining back the 0.4 dB of dynamic range loss. However, increasing the filter resistance to reduce bandwidth can have detrimental effects on THD performance, while the ADC driver may have difficulty driving larger capacitive loads. If additional filtering is required, the ADC driver can be configured to provide a filtering benefit.

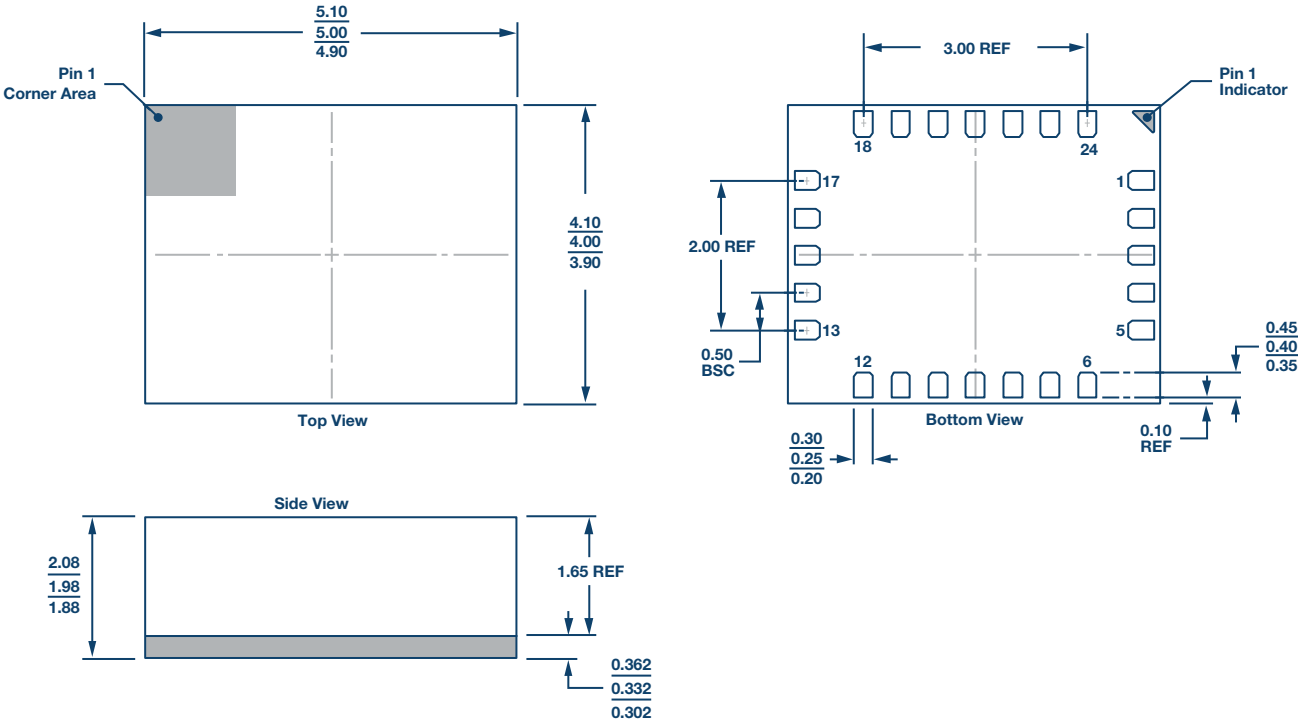

Figure 2. ADAQ798x package outline drawing.

Also included within the ADAQ798x products is a low noise, 2.5 V CMOS LDO linear regulator. Some SAR ADC products require a specific supply of 2.5 V with a small tolerance range. For users that do not have a 2.5 V supply rail available, one would have to be generated specifically for the ADC. With this component, the supplies have been greatly simplified as a result of the inclusion of the LDO. The onboard LDO is used to supply the converter and the LDO input now acts as the ADC supply. This provides a much wider range of usable supply voltages. It also provides a level of simplicity. The positive amplifier supply can be used as the LDO input to create a single-supply system. Additionally, the supply voltage choices can be made to optimize for performance or power consumption. The device features full power-down capability. The flexibility of the supply configurations allows the ADAQ798x user to make the trade-offs most appropriate for their application.

The ADAQ798x package dimensions are 5 mm × 4 mm × 2 mm. The four layer laminate is 0.35 mm thick, while the mold cap is 1.65 mm thick. This over-mold encapsulation features full mold compound and underfill just like any typical encapsulated integrated circuit. The laminate presents an LGA footprint to the user and features 24 I/O pads. Figure 2 shows the package outline drawing of the ADAQ798x. Figure 3 is a model of the ADAQ798x assembly without any encapsulation or mold compound. Figure 3 displays that the subsystem is a mix of Analog Devices active components and commonly available open market passive components. The laminate traces have been designed to control impedances and eliminate any crosstalk effects. The culmination of all these design and assembly techniques has led to the development of a product that can save up to 50% PCB area when compared to similar individual component designs.

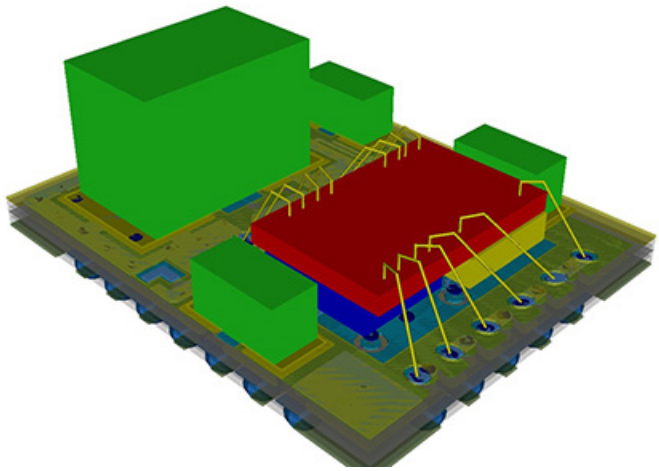

Figure 3. ADAQ798x 3D assembly model.

On top of the area savings, the ADAQ798x gives signal chain designers a better chance of achieving desired performance and reduces the risk of system redesign. Ultimately, this should lead to a shorter time to market and reduced development cost. The system bill of materials is also simplified by choosing the ADAQ798x and now more of the system is covered by one data sheet. This SiP component is robust. It is designed and extensively qualified to withstand harsh industrial environments. It delivers excellent quality ratings and is specified over a –55°C to +125°C temperature range. Overall, the ADAQ798x delivers an exceptional balance of integration vs. flexibility without compromising signal chain performance.

Ryan Curran [ryan.curran@analog.com] is a product applications engineer within the Precision Converters business unit at Analog Devices. He joined ADI in 2005 and has focused on SAR ADCs since joining the company. Ryan received his B.S.E.E. from the University of Maine in Orono, ME, and is currently pursuing an M.B.A. from the Isenberg School of Management at UMass Amherst.

Ryan Curran

Also by this Author:

RF-to-Bits Solution Offers Precise Phase and Magnitude Data for Material Analysis

Volume 48, Number 4