New Product Introduction:

64Mb-to-1Gb 1.8-V Quad SPI FS-S NOR Flash Memory Family

FS-S = Cypress's 1.8-V, 65-nm NOR Flash Memory Family With MirrorBit® Technology

The Industry's Fastest Quad SPI NOR Flash Memory Family for High-Performance Embedded Systems

High-Performance Systems Need Fast, Low-Pin-Count NOR Flash Memory

The market for 128Mb SPI NOR Flash Memory is projected to grow at a 20% CAGR, from 433M units in 2015 to 738M units in 2018[1]

128Mb 1.8-V SPI NOR Flash Memory market segments:

Automotive instrument clusters
Wearable electronics
Industrial controls
Home automation
Digital single-lens reflex (DSLR) cameras

Instrument Cluster in Audi TT

OEMs in these market segments design high-performance embedded systems that require fast NOR Flash Memory for both Program execution and data storage functions

Designers of high-performance systems prefer NOR Flash Memory with:

A low-pin-count serial interface to reduce package size and simplify board layout
The highest Read Bandwidth for Program Memory to keep the processor running at full speed
The fastest Program and Sector Erase speeds to quickly write data
Products that are AEC-Q100 qualified

Designers of high-performance systems require fast, low-pin-count Quad SPI NOR Flash Memory

[1] Source: iSuppli; market includes SPI and Quad SPI NOR Flash Memories

Cypress: No. 1 in NOR Flash, SRAM, NVRAM

Comparison to Competitors' Memory Product Portfolios

Product Category		Cypress	Competitors						Performance Advantage	Metrics
			ISSI	Micron	Toshiba	Winbond	Macronix	Fujitsu		
No. 1 NOR Flash	Parallel NOR Flash	✓	✓	✓		✓	✓		Highest Read Bandwidth Fastest Program/Erase	102 MBps
	Serial NOR Flash●	✓	✓	✓		✓	✓		Highest Read Bandwidth Fastest Program/Erase	160 MBps
	HyperFlash™[1]	✓	✓						Highest Read Bandwidth	333 MBps
No. 1 SRAM	QDR®-IV Synchronous SRAM	✓			✓				Highest RTR (random transaction rate)	2.1 GT/s
	Asynchronous SRAM with ECC[2]	✓	✓		✓				Highest reliability	<0.1 FIT[3]
	MicroPower SRAM	✓	✓						Lowest standby current	1.5 µA
No. 1 NVRAM	Serial F-RAM™[4]	✓						✓	Lowest standby current	100 µA
	Parallel nvSRAM[5]	✓							Fastest NVRAM[6]	20 ns
	AGIGARAM®[7]	✓							Highest-density NVRAM[6]	16GB

Cypress has the broadest portfolio of high-performance memories for embedded systems

[1] A Cypress NOR Flash Memory product family that offers higher bandwidth than Quad SPI NOR Flash Memory with one-third the number of pins of parallel NOR Flash Memory
[2] Error-correcting code
[3] Failures In Time (billion hours)
[4] Ferroelectric RAM
[5] Nonvolatile SRAM
[6] Nonvolatile memory that provides direct access to read and write to any memory location in any random order
[7] A Cypress brand name

● This presentation

NVM Problems Designers Face

1. **Systems require the highest Read Bandwidth for Program execution**
   Low Read Bandwidth is a major bottleneck to overall system performance
   Traditional 128Mb Quad SPI NOR Flash Memory products have typical Read Bandwidths of just 52 MBps

2. **High-performance systems require low-pin-count NOR Flash Memory**
   High-pin-count interfaces require a larger footprint and additional signal layers, increasing PCB cost
   Traditional 128Mb parallel-interface NOR Flash Memory requires a 56-pin package (280 mm^2) and a large PCB area

3. **Systems must have the fastest Program and Sector Erase times possible**
   Slow Program time decreases manufacturing throughput
   Traditional 128Mb Quad SPI NOR Flash Memory products are limited to a Program time of 0.5 ms per 256 bytes
   Systems must conduct a Sector Erase prior to programming new data into NOR Flash Memory
   Traditional 128Mb Quad SPI NOR Flash Memory products may have Sector Erase times as high as 700 ms

4. **Automotive applications also require AEC-Q100-qualified products**
   Traditional 128Mb Quad SPI NOR Flash Memory products are not AEC-Q100 qualified

Cypress's 128Mb Quad SPI NOR Flash Memory solves these problems by providing:

A Quad SPI interface NOR Flash Memory in either an 8-pin (48-mm^2) or 24-ball (48-mm^2) package to simplify board layout

An 80-MHz DDR mode with 80-MBps Read Bandwidth

A 0.36-ms Program time per 256 bytes

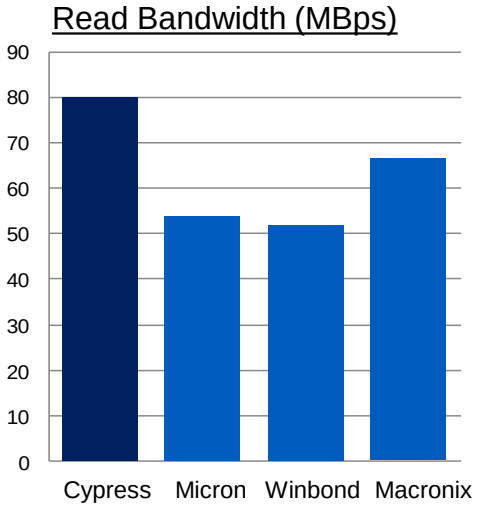
A 240-ms Sector Erase time

An AEC-Q100 qualification

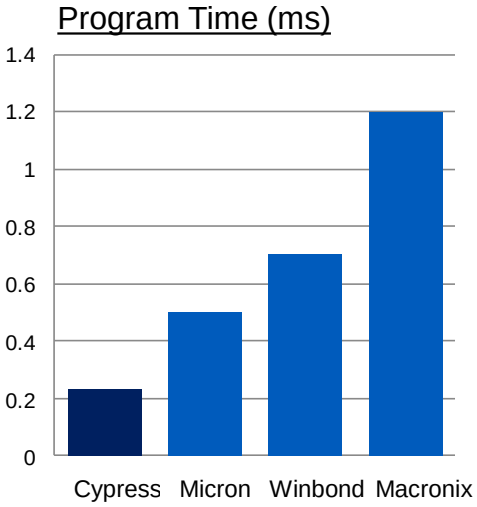
Cypress offers the industry's fastest 128Mb Quad SPI NOR Flash Memory for high-performance systems

Cypress Quad SPI NOR Flash Memory: The Industry's Fastest Solution

Cypress's NOR Flash Memory combines the industry's **highest** Quad SPI **Read Bandwidth**…



With the industry's **fastest SPI Program time**…



To produce the **highest-performance solutions** for high-performance applications.

Blade Server by HP

Cypress's 128Mb (FS128S) Quad SPI NOR Flash Memory

Applications

Automotive instrument clusters
Wearable electronics
Industrial controls
Home automation
Digital single-lens reflex (DSLR) cameras

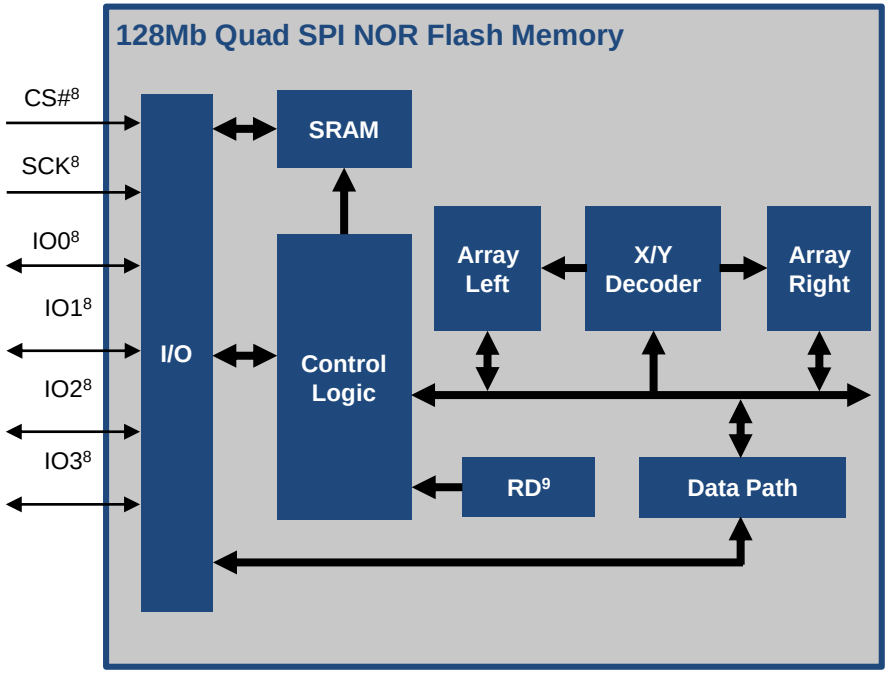
Features

Operating voltage range: 1.7 V to 2.0 V
100,000 Program[1]/Sector Erase[2] endurance cycles[3]
20-year data retention at +55°C
SDR[4] clock rate: 133-MHz QIO[5]
DDR[6] clock rate: 80-MHz QIO[5]
Program[1] time (256B): 0.36 ms (typical)
Sector Erase[2] time (64KB): 240 ms (typical)
Industrial temp range (AEC-Q100 optional): -40°C to +85°C
Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
Packages: 8-SOIC 208 mil, 8-WSON[7] 5 mm x 6 mm,
24-ball BGA 6 mm x 8 mm

Collateral

Datasheet: S25FS128S
App Notes: Cypress FS-S SPI NOR Flash Memory

Block Diagram



Availability

Sampling: Now
Production: Now

[1] The operation required to change a value "1" to a value "0" in NOR Flash Memory
[2] The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value "1"
[3] The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
[4] Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
[5] Quad input/output: An interface that transfers addresses or data on four I/Os simultaneously
[6] Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
[7] Very, Very Thin, Small-Outline, No-Lead semiconductor package
[8] Signals used for standard Quad (x4) SPI interface. Refer to the S25FS128S datasheet for signal definitions in the x1 and x2 mode.
[9] Read data buffer

SPI NOR Flash Memory Portfolio

	S25FL2-K[1] 90 nm, 3.0 V 4KB[2]	S25FL1-K 90 nm, 3.0 V 4KB[2]	S25FL-L 65 nm, 3.0 V 4KB[2]	S25FL-P 90 nm, 3.0 V >4KB[2]	S25FL-S 65 nm, 3.0 V >4KB[2]	S79FL-S[3] 65 nm, 3.0 V >4KB[2]	S25FS-S 65 nm, 1.8 V >4KB[2]
≥256Mb	**Density** SDR Clock / DDR Clock * Temp Range All parts supported by Longevity Program unless noted		**256Mb** Q416 133 MHz / 66 MHz * I, A, V, B, N, M	**256Mb**[5] 104 MHz / -- * I, A	**1Gb**[5] 133 MHz / 80 MHz * I, A, V, B **512Mb** 133 MHz / 80 MHz * I, A, V, B **256Mb** 133 MHz / 80 MHz * I, A, V, B, N, M	**1Gb** 133 MHz / 80 MHz * I, A, V, B **512Mb** 133 MHz / 80 MHz * I, A, V, B **256Mb** 133 MHz / 80 MHz * I, A, V, B	● **1Gb**[5] 133 MHz / 80 MHz * I, A, V, B ● **512Mb** 133 MHz / 80 MHz * I, A, V, B ● **256Mb** 133 MHz / 80 MHz * I, A, V, B
64-128Mb		**64Mb** 108 MHz / -- * I, A, V, B, N[4], M[4]	**128Mb** 133 MHz / 66 MHz * I, A, V, B, N, M **64Mb** 108 MHz / 54 MHz * I, A, V, B, N, M	**128Mb**[6] 104 MHz / -- * I, A, V, B **128Mb**[7] 104 MHz / -- * I, A, V, B **64Mb** 104 MHz / -- * I, A, V, B	**128Mb**[8] 133 MHz / 80 MHz * I, A, V, B, N, M **128Mb**[9] 108 MHz / -- * I, A, V, B		● **128Mb** 133 MHz / 80 MHz * I, A, V, B ● **64Mb** 133 MHz / 80 MHz * I, A, V, B, N, M
≤32Mb	**8Mb** Q117 76 MHz / -- * I	**32Mb** 108 MHz / -- * I, A, V, B, N[4], M[4] **16Mb** 108 MHz / -- * I, A, V, B, N[4], M[4]		**32Mb** 104 MHz / -- * I, A, V, B			

* I = Industrial: -40°C to +85°C
A = Industrial, AEC-Q100: -40°C to +85°C
V = Industrial-plus: -40°C to +105°C
B = Industrial-plus, AEC-Q100: -40°C to +105°C
N = Extended: -40°C to +125°C
M = Extended, AEC-Q100: -40°C to +125°C

[1] S25FL2-K Dual SPI
[2] Logical sector size
[3] S79 series, Dual Quad SPI (stacked die)
[4] Contact Sales
[5] S70 series (stacked die)
[6] S25FL129P Quad SPI
[7] S25FL128P Dual SPI
[8] S25FL128S 133-MHz SDR / 80-MHz DDR
[9] S25FL127S 108-MHz SDR

Status: Concept, Development, Sampling, Production
Availability: QQYY
EOL (Last-Time-Ship): QQYY
● This presentation

Here's How to Get Started

1. **Download our datasheet: S25FS256S**

2. **Download our app notes: Cypress FS-S SPI NOR Flash Memory**

3. **Register to access online technical support**

4. **Contact Cypress for more information**

Thermostat
by Nest

Wearable
by Sensoplex

References and Links

Product Website:

www.cypress.com/FS-S-Website

S25FS-S Datasheets:

www.cypress.com/S25FS064S-Datasheet
www.cypress.com/S25FS128S-Datasheet
www.cypress.com/S25FS256S-Datasheet
www.cypress.com/S25FS512S-Datasheet
www.cypress.com/S70FS01GS-Datasheet

Application Notes:

www.cypress.com/FS-S-App-Note

Design Models:

www.spansion.com/Products/memory/Serial-Flash/Pages/Spansion-FS.aspx

Drivers and Software:

www.cypress.com/sdc

Product Selector Guide, Cross Reference Guide and Tool:

www.spansion.com/Products/Pages/ProductFinder.aspx
www.spansion.com/Brochures/Spansion_Cross_Reference_Guide.pdf
www.spansion.com/Products/Pages/CompetitorCrossReference.aspx

Hardware Development Tools:

www.cypress.com/cypress-store

APPENDIX


Detector - PSoC Creator 2.0
DAC
LCD Drive
ADC
CapSense
PGA
PWM
MCU
Amplifier
nvSRAM
Timer
UART
Counter
Custom Logic
Filter
HV IOs
MR
8051
ARM
Cortex-M3
Wireless
USB
CAN

NOR Flash Memory Terms

Nonvolatile Memory (NVM)

A memory that retains data even when it is not powered

Program

A **low-latency**, high-bandwidth NVM that enables fast execution of CPU instructions

Flash Memory

An NVM that alters the voltage at which a transistor conducts current by adding or removing electrons to set predefined "1" and "0" states for a memory cell

NOR Flash Memory

A Flash Memory with a memory architecture optimized for fast, **low-latency** random access (vs. fast consecutive address access)

MirrorBit®

Cypress NVM cell technology with two localized electron storage locations to provide two data bits per cell, effectively doubling the NOR Flash Memory density

Read Bandwidth

The measurement of how fast data can be read from a memory, expressed in bytes per second

Serial Peripheral Interface (SPI)

An industry-standard, low-pin-count interface used in embedded systems that enables synchronous data exchange (1 bit per cycle) between a master and slave device(s)

Quad SPI

An industry-standard, high-bandwidth, low-pin-count interface that simultaneously uses a four-wire SPI interface to enable faster data transactions

Additional NOR Flash Memory Terms

Single-Data-Rate (SDR)

A mode of data transfer in which data is transferred once per clock cycle

Double-Data-Rate (DDR)

A mode of data transfer in which data is transferred twice per clock cycle

Program/Erase

The operation required to change a NOR Flash Memory cell state from “1” to “0” or from “0” to “1”, respectively

Sector

A physical block of memory locations with consecutive addresses (e.g., a 4KB sector in a 256Mb memory)

Sector Erase

The operation in which all the bytes in a Sector of NOR Flash Memory are Erased simultaneously prior to Programming

Chip Erase

The operation in which all memory cells in the NOR Flash Memory are Erased prior to Programming

Cypress's 64Mb (FS064S) Quad SPI NOR Flash

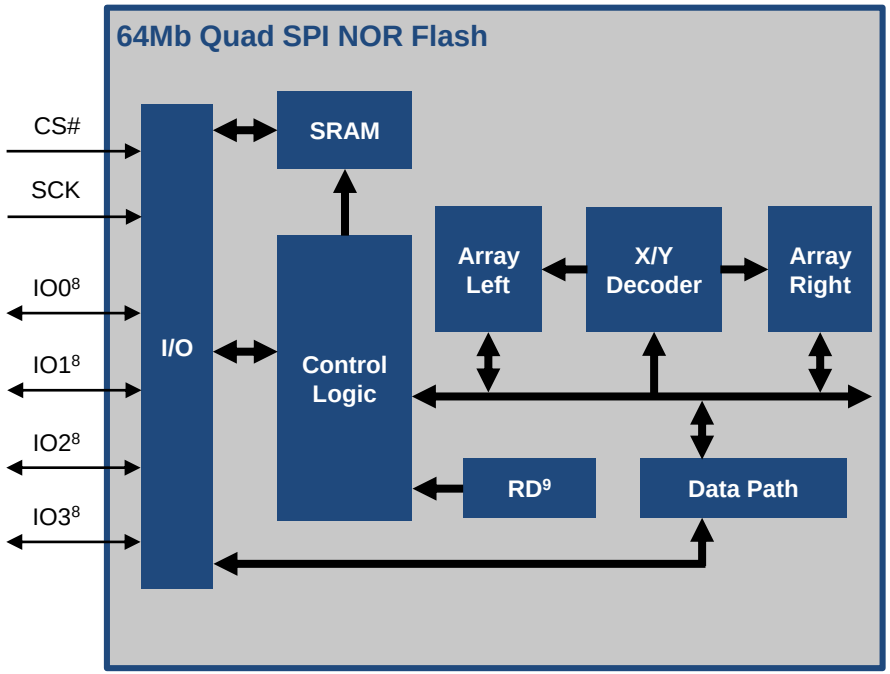
Applications

Bluetooth/wireless devices
Consumer electronics
Communications equipment

Features

Operating voltage range: 1.7 V to 2.0 V
100,000 Program[1]/Block Erase[2] endurance cycles[3]
20-year data retention at +55°C
SDR[4] speed: 133-MHz QIO[5]
DDR[6] speed: 80-MHz QIO[5]
Program[1] time (256B): 0.36 ms (typical)
Block Erase[2] time (64KB): 145 ms (typical)
6-µA Deep power-down[7] Current (typical)
Industrial temp range (AEC-Q100 optional): -40°C to +85°C
Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
Extended temp range: -40°C to +125°C
Packages: 8-SOIC 208 mil, 24-ball BGA 6 mm x 8 mm,
8-contact LGA 5mm x 6mm

Block Diagram



Collateral

Datasheet: S25FS064S
App Notes: Cypress FS-S SPI NOR Flash Memory

Availability

Sampling: Now
Production: Now

[1] The operation required to change a value "1" to a value "0" in NOR Flash
[2] The operation required prior to a NOR Flash Program, in which all the bits in a block (64KB) are set to value "1"
[3] The number of times a NOR Flash memory cell can be Programmed or Erased before it wears out
[4] Single data rate: A mode of data transfer in which the commands, addresses or data inputs are transferred on the rising edges of the clock signal
[5] Quad input/output: An interface that uses four bits simultaneously to transfer address and data
[6] Double data rate: A mode of data transfer in which commands, addresses or data inputs are transferred on both the rising and falling edges of the clock signal
[7] A power saving mode in which all sense amps and peripheral circuits are turned off
[8] Signals used for standard Quad (x4) SPI interface; refer to the S25FS064S datasheet for signal definitions in the x1 and x2 mode
[9] Read data buffer

Cypress's 256Mb (FS256S) Quad SPI NOR Flash Memory

Applications

Wearable electronics
Advanced driver assistance systems (ADAS)
Portable communications, Wireless LAN
Blade server
Road tolling system

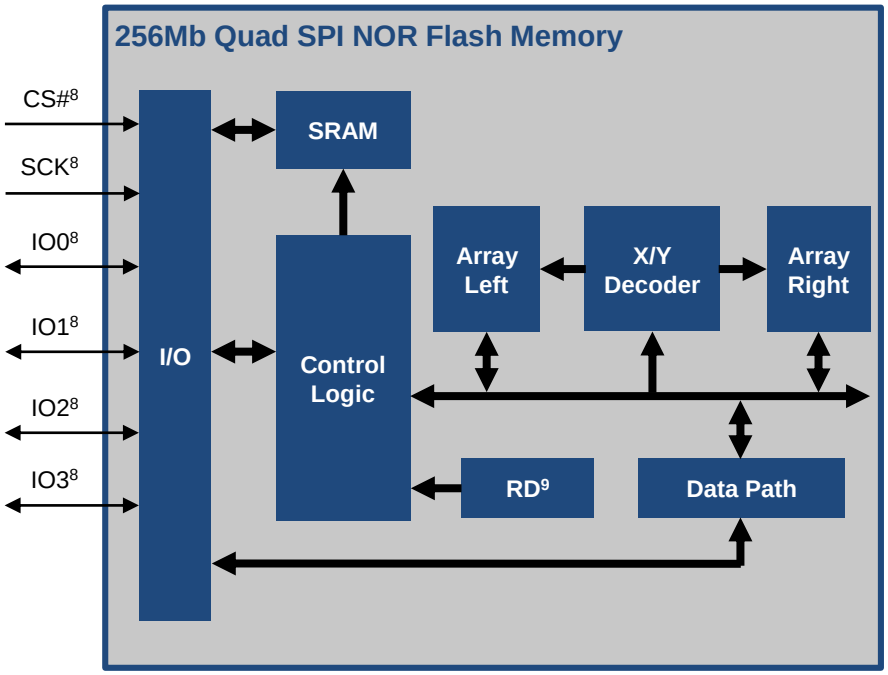
Features

Operating voltage range: 1.7 V to 2.0 V
100,000 Program[1]/Sector Erase[2] endurance cycles[3]
20-year data retention at +55°C
SDR[4] clock rate: 133-MHz QIO[5]
DDR[6] clock rate: 80-MHz QIO[5]
Program[1] time (256B): 0.360 ms (typical)
Sector Erase[2] time (64KB): 240 ms (typical)
Industrial temp range (AEC-Q100 optional): -40°C to +85°C
Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
Packages: 16-SOIC 300 mil, 8-WSON[7] 6 mm x 8 mm,
24-ball BGA 6 mm x 8 mm

Collateral

Datasheet: S25FS256S
App Notes: Cypress FS-S SPI NOR Flash Memory

Block Diagram



Availability

Sampling: Now
Production: Now

[1] The operation required to change a value "1" to a value "0" in NOR Flash Memory
[2] The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value "1"
[3] The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
[4] Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
[5] Quad input/output: An interface that transfers addresses or data on four I/Os simultaneously
[6] Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
[7] Very, Very Thin, Small-Outline, No-Lead semiconductor package
[8] Signals used for standard Quad (x4) SPI interface; refer to the S25FS256S datasheet for signal definitions in the x1 and x2 mode
[9] Read data buffer

Cypress's 512Mb (FS512S) Quad SPI NOR Flash Memory

Applications

Wearable electronics
Automotive telematics/infotainment
Advanced driver assistance systems (ADAS)
Networking/communications, e.g., base station, WiFi, Long Term Evolution (LTE)

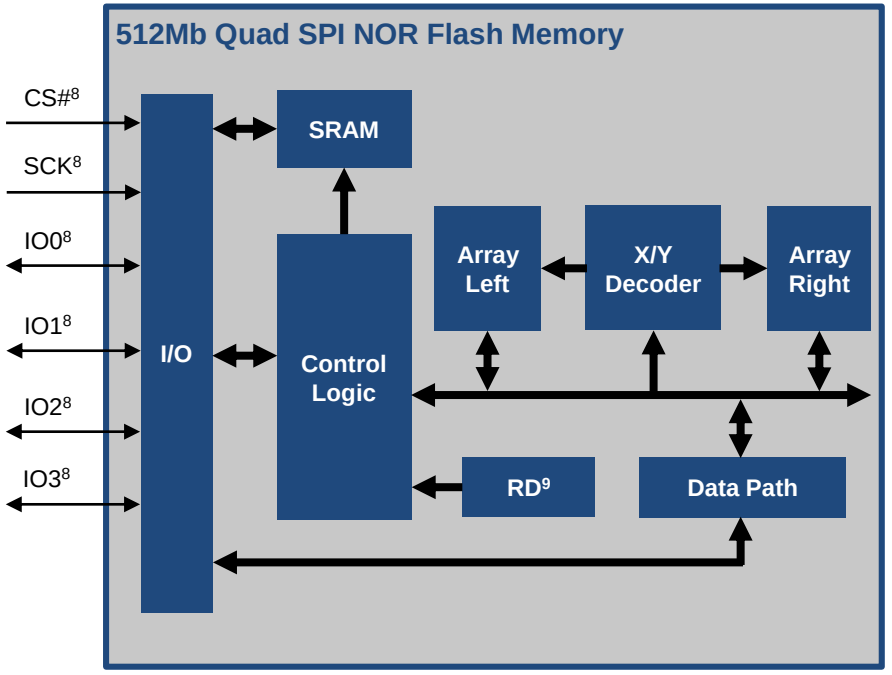
Features

Operating voltage range: 1.7 V to 2.0 V
100,000 Program[1]/Sector Erase[2] endurance cycles[3]
20-year data retention at +55°C
SDR[4] clock rate: 133-MHz QIO[5]
DDR[6] clock rate: 80-MHz QIO[5]
Program[1] time (512B): 0.360 ms (typical)
Sector Erase[2] time (256KB): 930 ms (typical)
Industrial temp range (AEC-Q100 optional): -40°C to +85°C
Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
Packages: 16-SOIC 300 mil, 8-WSON[7] 6 mm x 8 mm, 24-ball BGA 6 mm x 8 mm

Collateral

Datasheet: S25FS512S
App Notes: Cypress FS-S SPI NOR Flash Memory

Block Diagram



Availability

Sampling: Now
Production: Now

[1] The operation required to change a value "1" to a value "0" in NOR Flash Memory
[2] The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value "1"
[3] The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
[4] Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
[5] Quad input/output: An interface that transfers addresses or data on four I/Os simultaneously
[6] Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
[7] Very, Very Thin, Small-Outline, No-Lead semiconductor package
[8] Signals used for standard Quad (x4) SPI interface. Refer to the S25FS512S datasheet for signal definitions in the x1 and x2 mode.
[9] Read data buffer

Cypress's 1Gb (FS01GS) Quad SPI NOR Flash Memory

Applications

Base stations
Home gateways
Automotive telematics
Wireless LAN

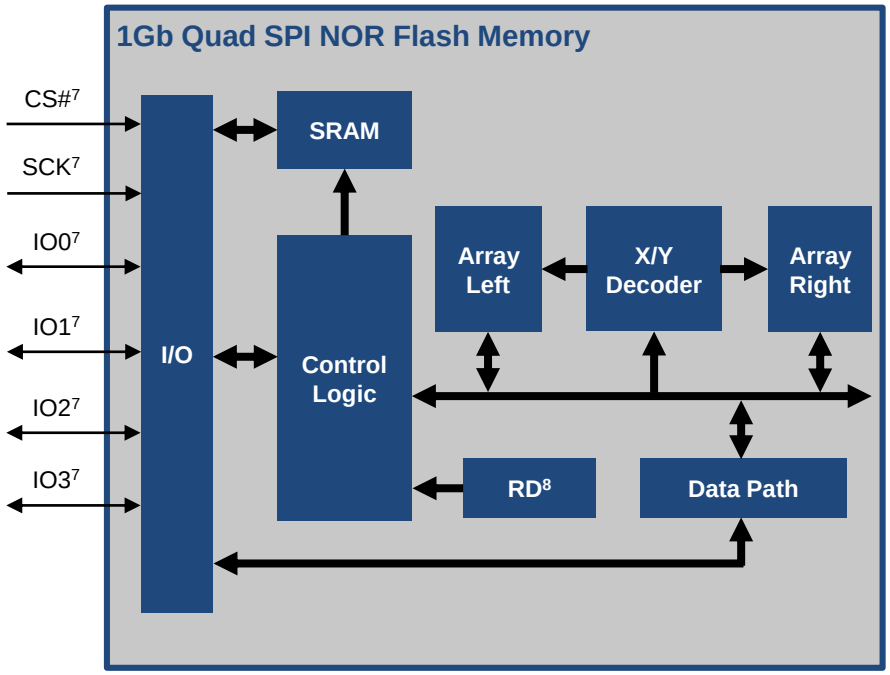
Features

Operating voltage range: 1.7 V to 2.0 V
100,000 Program[1]/Sector Erase[2] endurance cycles[3]
20-year data retention at +55°C
SDR[4] clock rate: 133-MHz QIO[5]
DDR[6] clock rate: 80-MHz QIO[5]
Program[1] time (512B): 0.340 ms (typical)
Sector Erase[2] time (256KB): 520 ms (typical)
Industrial temp range (AEC-Q100 optional): -40°C to +85°C
Industrial-plus temp range (AEC-Q100 optional): -40°C to +105°C
Packages: 16-SOIC 300 mil, 24-ball BGA 6 mm x 8 mm

Collateral

Datasheet: S70FS01GS
App Notes: Cypress FS-S SPI NOR Flash Memory

Block Diagram



Availability

Sampling: Now
Production: Now

[1] The operation required to change a value "1" to a value "0" in NOR Flash Memory
[2] The operation required prior to a NOR Flash Memory Program, in which all the bits in a Sector are set to value "1"
[3] The number of times a NOR Flash Memory Sector can be Programmed/Erased before it wears out
[4] Single-data-rate: A mode of data transfer in which data is transferred once per clock cycle
[5] Quad input/output: An interface that transfers addresses or data on four I/Os simultaneously
[6] Double-data-rate: A mode of data transfer in which data is transferred twice per clock cycle
[7] Signals used for standard Quad (x4) SPI interface
[8] Read data buffer

Serial NOR Flash Memory Product Selector Guide

S25/70FS-S Part Numbering Decoder

S XXFSYYYS AG M F I 00 0

Packing Type:	0 = Tray, 1 = Tube (for SOIC/WSON only), 3 = 13″ Tape & Reel
Model Number:	SOIC (8-pin or 16-pin)/WSON (6 mm x 5 mm or 6 mm x 8 mm) BGA (5x5 ball or 4x6 ball)/8-pin SOIC DDR
Temperature Range:	I = Industrial: -40°C to +85°C A = Industrial, AEC-Q100: -40°C to +85°C V = Industrial-plus: -40°C to +105°C B = Industrial-plus, AEC-Q100: -40°C to +105°C N = Extended: -40°C to +125°C
Package Material:	F = Lead (Pb)-Free (for SOIC/WSON only) H = Low-Halogen, Lead (Pb)-Free (for BGA only)
Package Type:	M = SOIC, N = WSON, B = BGA 6x8
Performance:	AG = 133-MHz Multi-I/O, DS = 80-MHz DDR
Base MPN:	XX = 25, YYY = 64 64Mb MirrorBit Serial Flash Memory XX = 25, YYY = 128 128Mb MirrorBit Serial Flash Memory XX = 25, YYY = 256 256Mb MirrorBit Serial Flash Memory XX = 25, YYY = 512 512Mb MirrorBit Serial Flash Memory XX = 70, YYY = 01G 1Gb Dual Die Stack MirrorBit Serial Flash Memory
Spansion	