

GROWHOUSE - IOT GATEWAY

MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	0.1	Created Initial Draft	21/09/2018
	0.5	Schematic Released for External Review	16/11/2018
	1.0	PCB Released To Fabrication	09/01/2019
2.0	2.0	Beta PCB Released To Fabrication	31/07/2019

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PAGE 02 : BLOCK DAIGRAM

PAGE 03 : EXPANSION CONNECTORS

PAGE 04 : USB TO ETHERNET

PAGE 05 : ZIGBEE MODULE

PAGE 06 : REVISION HISTORY

PCB LAYER STACK-UP DETAILS

Layer	Stack up	Supplier	Type	Description	Base Thickness	Finish Thickness	Copper Coverage	oz
1		Electra	Soldermask	Electra - EMI110 Glossy				4.000
		Circuit Foil	Copper	0.5 oz copper foil	0.660	1.860	0.000	
		Isola	Dielectric	Isola 370HR Prepreg 106	2.300	1.500		3.740
		Isola	Dielectric	Isola 370HR Prepreg 1080	3.000	2.500		3.900
2					1.299	1.299	60.000	
		Isola	Core	47 mil 1/1 370HR	47.000	47.000		4.470
					1.299	1.299	30.000	
		Isola	Dielectric	Isola 370HR Prepreg 1080	3.000	2.500		3.900
3		Isola	Dielectric	Isola 370HR Prepreg 106	2.300	1.500		3.740
		Circuit Foil	Copper	0.5 oz copper foil	0.660	1.860	0.000	
		Electra	Soldermask	Electra - EMI110 Glossy				4.000

Copper Thickness - 8.318 | Dielectric Thickness - 54.870 | Solder Mask Thickness - 2.400 | Stack Up Thickness - 61.188 | Stack Up Thickness with Soldermask - 63.588 | Stack Up Cost = 3.00 |

PCB MECHANICAL DETAILS :

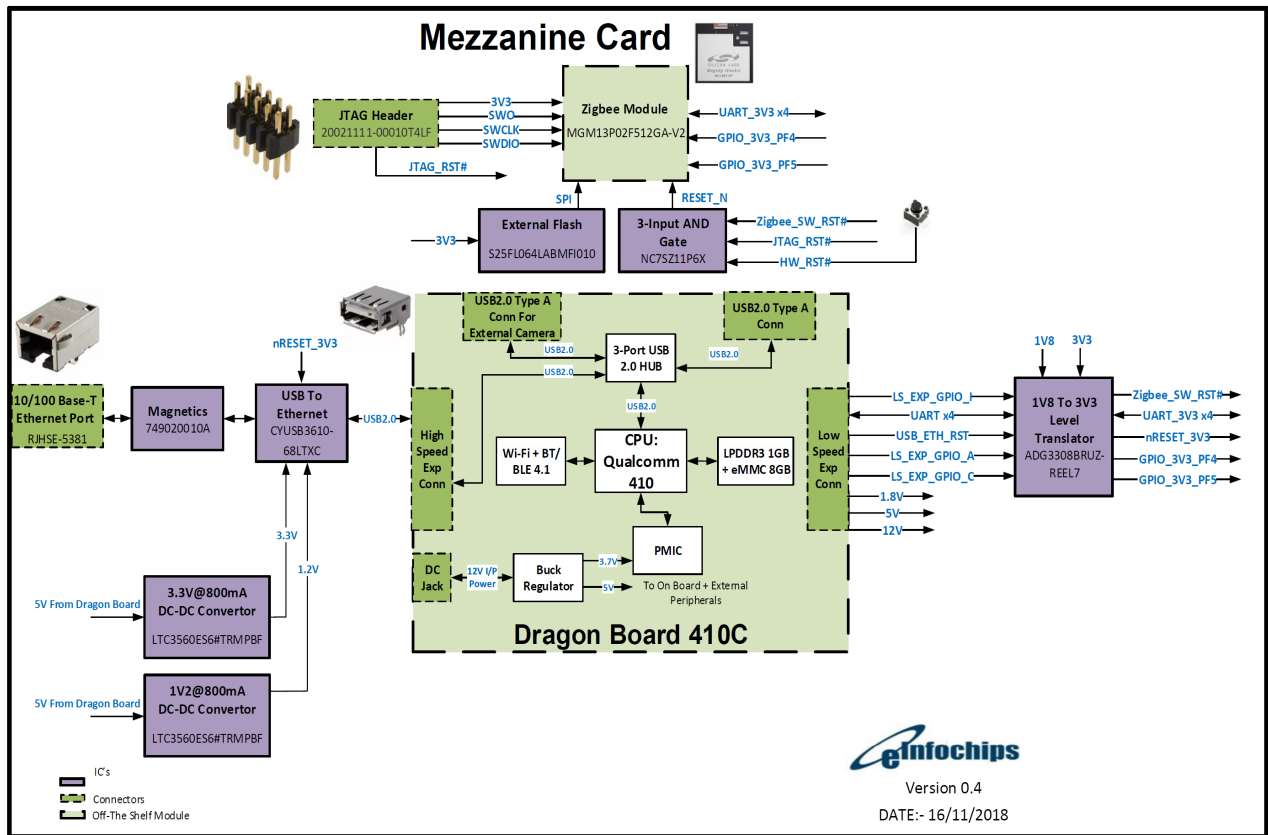
1. PCB SIZE: 77 MM x 54 MM
2. PCB MATERIAL: FR-4
3. NUMBER OF LAYERS: 4
4. IMPEDANCE CONTROL: YES

NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'DNP'.
4. SIGNAL NET NAMES WITH "_" SUFFIX, ARE ACTIVE LOW SIGNALS.
5. RESISTORS ARE OF 0402 SIZE AND 5% TOLERANCE UNLESS SPECIFIED OTHERWISE
6. CAPACITORS ARE OF 0402 SIZE UNLESS SPECIFIED OTHERWISE
7. ALL THE PARTS INDUSTRIAL TEMPERATURE GRADE.

Project		Designed eInfochips	
IOT GATEWAY		 The Solutions People	
Title			
COVER PAGE			
Size C	eInfochips#: 16_00675_02		Rev 2.0
Date: Monday, August 12, 2019		Sheet 1 of 6	

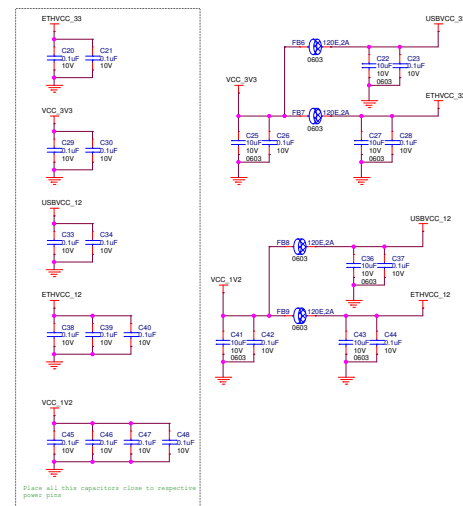
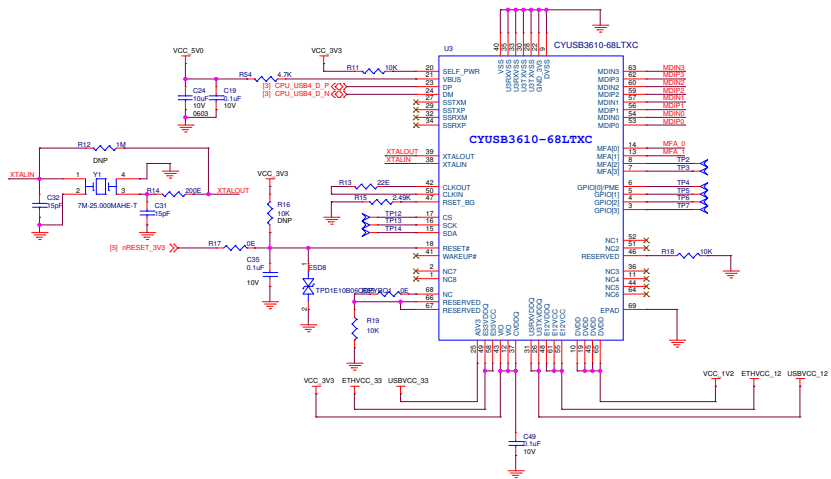
BLOCK DIAGRAM



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BLOCK DIAGRAM			
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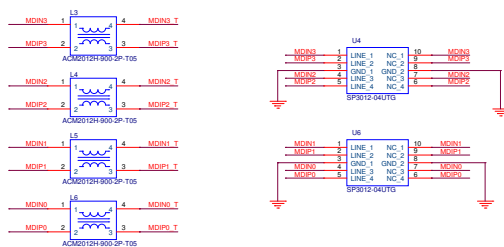
USB3.0 TO GIGABIT ETHERNET CONTROLLER

POWER SUPPLY

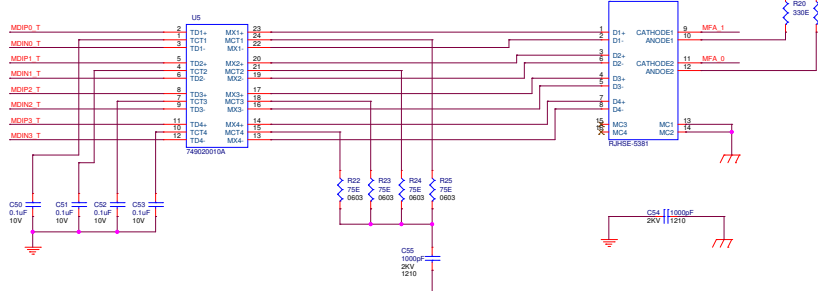


EMI PROTECTION

ESD PROTECTION

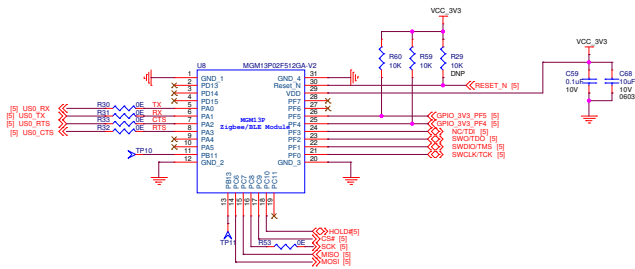


MAGNETICS & RJ45 ETHERNET PORT

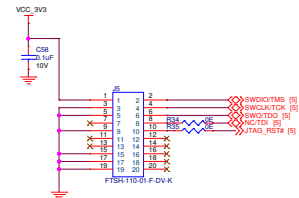


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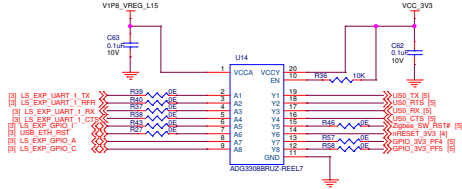
ZIGBEE/BLE MODULE



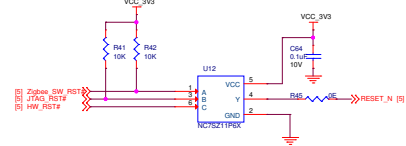
JTAG INTERFACE



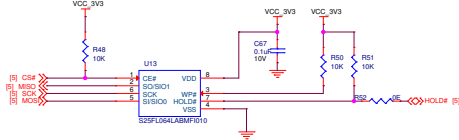
1.8V TO 3.3V LEVEL TRANSLATOR



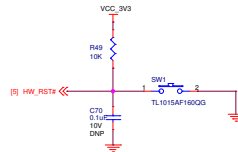
3-INPUT AND GATE



SPI FLASH FOR OTA UPGRADE



HARDWARE RESET



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ZIGBEE MODULE			
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REVISION HISTORY

PCB REV	SCH REV	CHANGE DESCRIPTION	DATE
1.0	0.1	- Created Initial Draft	19/09/2018
	0.2	- Changed the USB To Ethernet Microchip Part# LAN7500 U3 to the Cypress part# CYUSB3610 - Changed the U1 & U2 part to LTC3560ES6#TRMPBF as per the new cypress part - Changed the U13 part to IS25LQ040B-JNLE as it is proven with EFR32 series controller for OTA upgrade.	16/10/2018
	0.3	- Added Reset (SW3) & Power (SW2) Switch on Mezaanine Card to debug 410C Dragon Board - Added Series Resistor R54 of 4.7K value on VBUS input Pin#21 of U3. - Added TP's on EEPROM Singals of U3. - Added 0E Resistor on Pin# 68 of U3.	29/10/2018
	0.4	- Added Standard 2.1 mm DC Jack as dummy part	05/11/2018
	0.5	- Changed U11 part to ADG3308BRUZ-REEL7 from NLSX5014MUTAG & removed U9 from the design - Changed U13 part to S25FL064LABMF1010 from IS25LQ040B-JBLE	16/11/2018
	0.6	- Added Factory Reset Switch SW4 on GPIO_69 of Q410 Processor & its discretes in the design as per F/W team feedback	03/12/2018
	1.0	- PCB Released to Fabrication	09/01/2019
2.0	1.1	- Added ESD8 on reset line of U3 - U4, U6 & C35 is DNP in Alpha schematic, need to populate in beta schematic for ESD perouse	18/07/2019
	1.2	- Change the ESD8 part# to TPD1E10B06QDPYRQ1	23/07/2019
	2.0	- Board Released for Fabrication	31/07/2019

Project IOT GATEWAY		Designed elinfochips	
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