Application Note AN 2012-04
V1.0 April 2012

Cooling of thinPAK 8x8

IFAT PMM
Peinhopf Wolfgang

Edition 2011-02-02
Published by
Infineon Technologies Austria AG
9500 Villach, Austria

Attention please!

THE INFORMATION GIVEN IN THIS APPLICATION NOTE IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office. Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

AN 2012-04

Revision History: date (12-04-05) , V1.0

Authors: Wolfgang Peinhopf, application engineering, IFAT PMM APS SE PC

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: [wolfgang.peinhopf@infineon.com]

Table of contents

1 Introduction

For discrete high voltage MOSFETs dominating packages are through-hole-packages (THD) like the TO-220 or the TO-247. These packages offer very efficient cooling by attaching a heatsink directly to the large, exposed copper tab of the package. But these packages are quite big in size and have the drawback of significant package parasitics (i.e.: source inductivity). Alternatively, one could use a surface mount package like the D^{2}PAK. This package is also quite bulky and has due to the leads a high source inductivity value. The new package ThinPAK 8x8 with 1 mm package height offers a significant shrink in package size for same R_{DSon} values and is a leadless package with almost no source inductivity. To enable high level of power dissipation an efficient bottom side cooling system through the exposed drain pad has to be employed. To support system designers this application note describes the thermal characteristics of the ThinPAK 8x8 and an efficient way to cool the package through the exposed drain pad.

2 ThinPAK 8x8 package

The ThinPAK 8x8 package significantly reduces the package size compared to traditional packages like the D^{2}PAK (Fig. 1). This enables designers to shrink system size and to increase the power density. The package is leadless and offers almost no package source inductivity. The main cooling path is through the exposed metal drain pad to the PCB.

Characteristics:

- Small footprint (64 mm² vs. 150 mm² for D^{2}PAK)
- Low profile package (1.0 mm vs. 4.4 mm for D^{2}PAK)
- Low source inductance (2 nH vs. 6 nH for D^{2}PAK)
- Separate driver source connection
- Thermal performance similar to D^{2}PAK

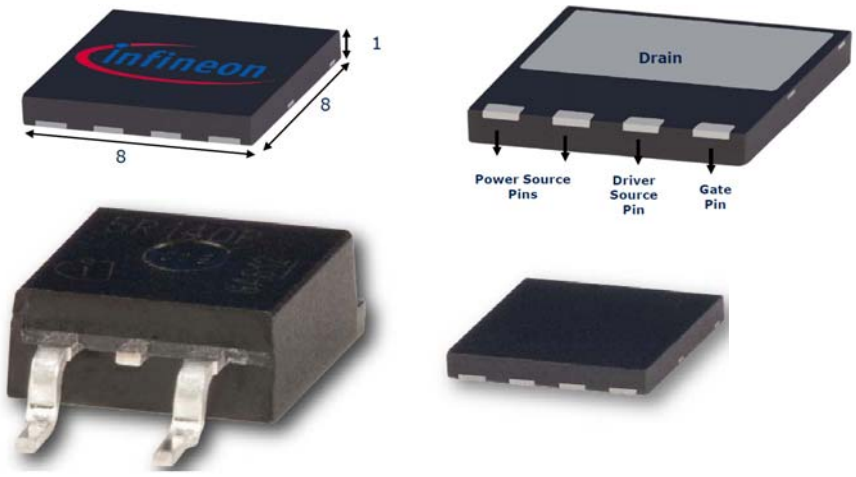

Fig. 1: ThinPAK 8x8 (8 x 8 x 1 mm³) vs. D^{2}PAK (10 x 15 x 4.4 mm³)

3 Cooling system: bottom side cooling

For SMD packages the PCB acts as a heatsink. The thermal performance is mainly determined by the copper area on the PCB and the number of layers. To improve the thermal performance the convective area to transfer the heat to the ambient air has to be increased. This can be done using a heatsink.

The heatsink is attached to the bottom side of the PCB. To cover height differences and roughness a thermal interface material (TIM) between the PCB and the heatsink is used. For efficient heat conduction through the PCB to the heatsink the thermal conduction resistance through the PCB must be reduced using thermal vias. Depending on the numbers of vias and the plating thickness of the vias the conduction resistance is in the range 1 – 3 K/W (see Fig. 2).

Comparing D^{2}PAK and ThinPAK 8x8 one has to consider that the exposed leadframe area of the D^{2}PAK is larger and the copper thickness is bigger. A thicker leadframe results in a higher thermal package resistance Rthjc (datasheet value) but it also improves the lateral heat conduction (heat spreading) which in turn increases the effective heat conduction area through the TIM to the heatsink. Fig. 4 shows clearly that the thermal resistance of the TIM is lower for the D^{2}PAK compared to the ThinPAK (difference in example: 1.25 K/W).

Fig. 5 shows the dependency of the thermal resistance from the junction point to the TIM depending on the number of vias (via pitch) and the plating thickness of the vias. In the shown example the bigger lever comes from via plating. One can also see that at ~ 35 µm via plating a further increase of the plating doesn't result in a huge benefit of the thermal performance.

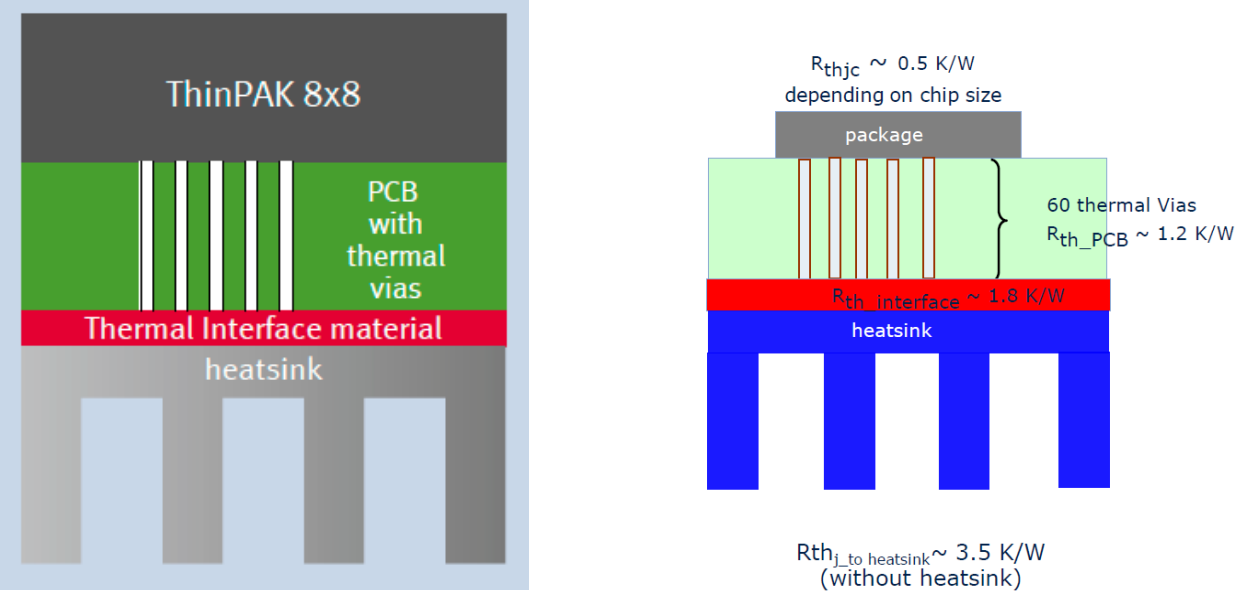

Fig. 2: Bottom side cooling system

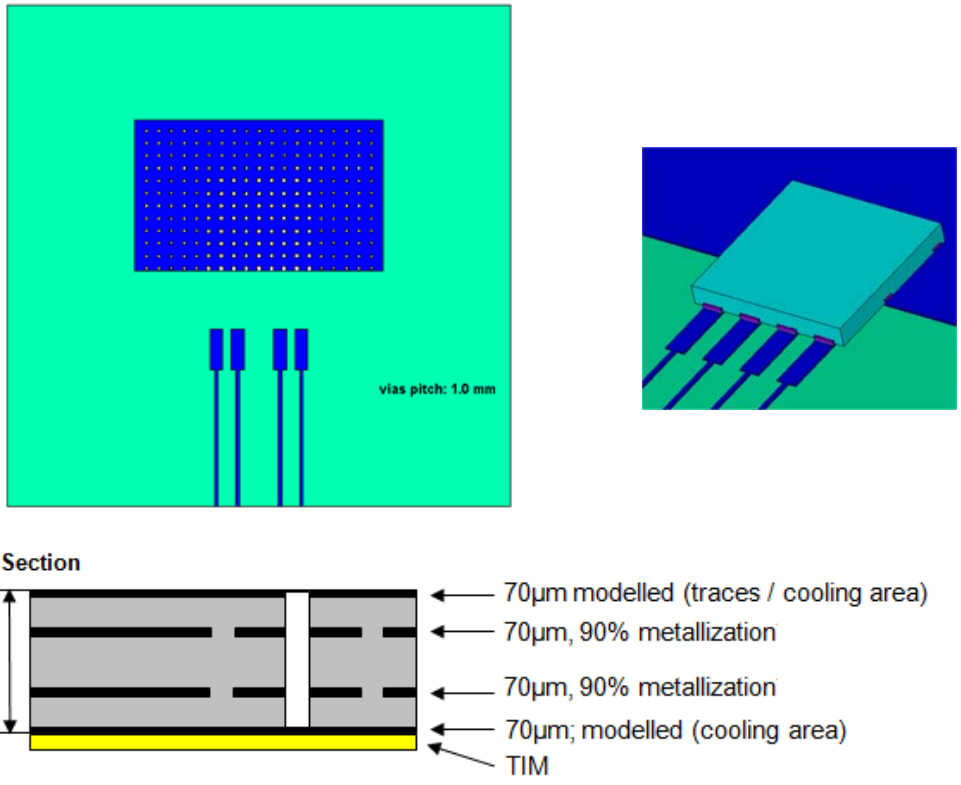

Fig. 3: PCB for thermal simulation (via pitch: 1.0 mm, 0.8 mm, 70 µm Cu, Cu area: 13 x 20 = 260 mm², 4 layer PCB, 1 mm thickness)

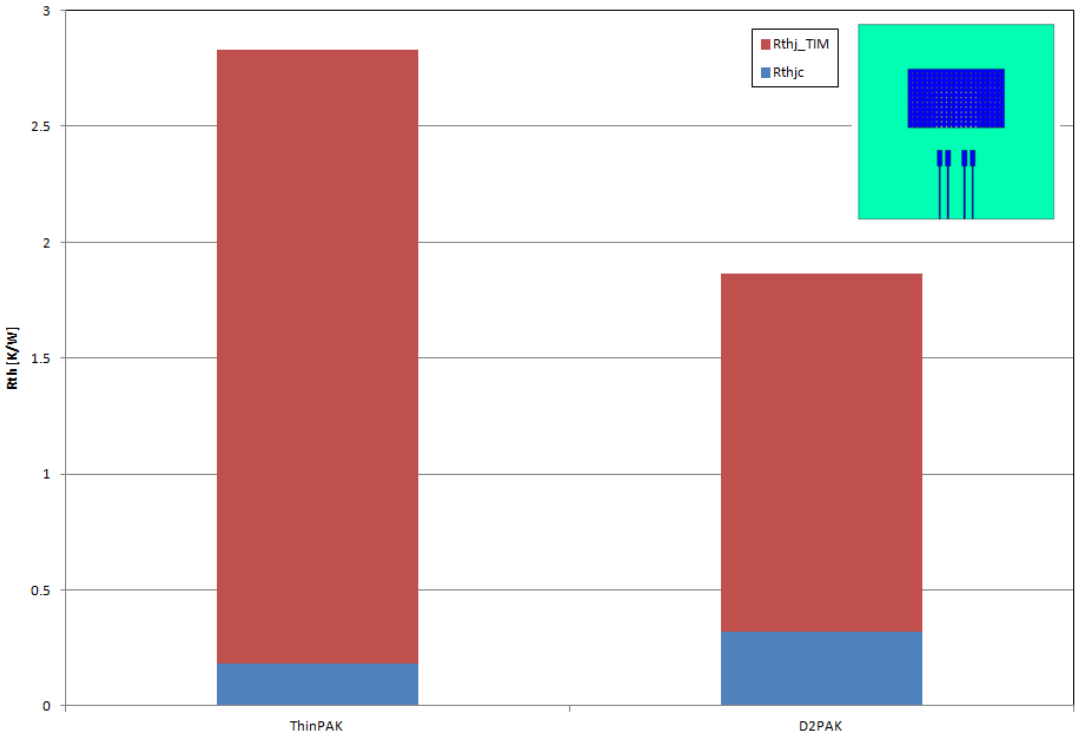

Fig. 4: Simulation Rth for ThinPAK and D^{2}PAK (TIM: thermal interface material, via pitch 0.8 mm, via plating 35 µm, PCB see Fig. 3)

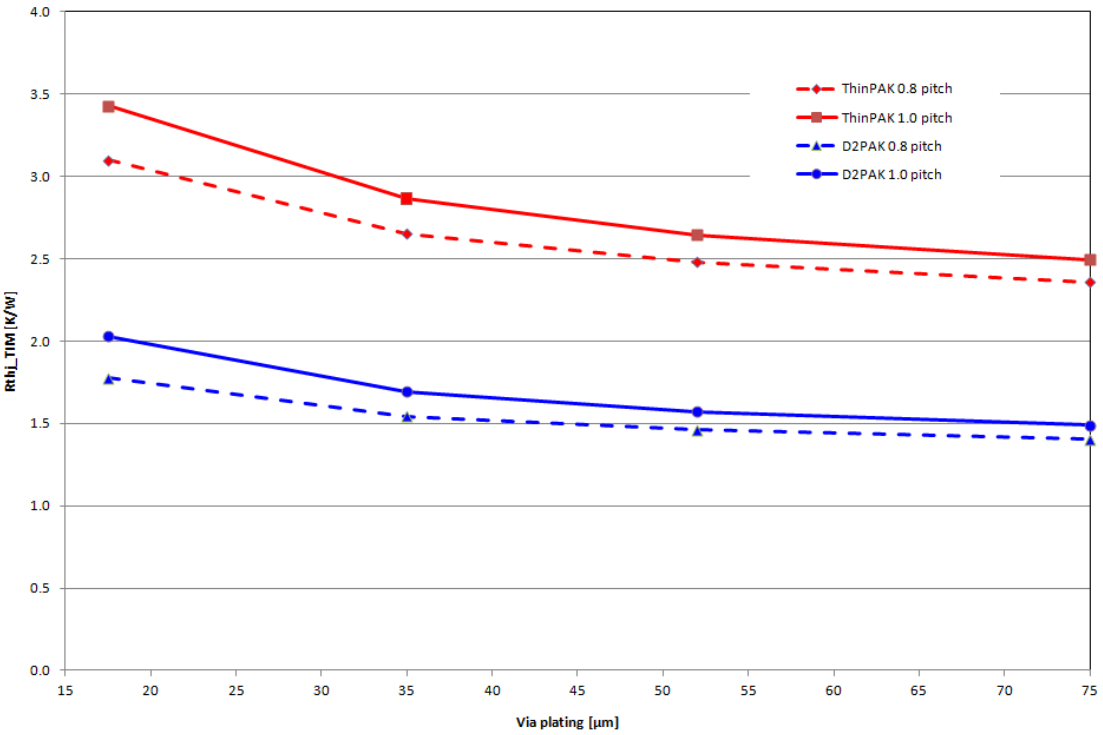

Fig. 5: Rth Simulation for ThinPAK and D^{2}PAK (TIM: thermal interface material, via pitch 0.8 mm, via plating 35 µm)

4 Measurement and simulation examples

To determine how much power can be transferred to the environment one has to consider the thermal resistance Rthja (junction to ambient). Fig. 6 shows a simulation for a low performance board with different copper areas. For min. footprint ThinPAK is approx. double as high as D^{2}PAK. Increasing the Cu area to 300 or 600 mm² improves this ratio to ~ 30%. The advantage for the D^{2}PAK comes from thicker and larger copper leadframe.

Using a better performing PCB the ThinPAK becomes better. Fig. 7 shows an example of a 4 layer board with vias. Using a smaller number of vias for ThinPAK (15 vs. 35 vias) the difference is ~ 30%. Using the same via count (35 vias) the difference reduces to 15%. Fig. 8 shows a measurement example with the same number of vias. The difference is ~ 10%.

In conclusion this means that utilizing the ThinPAK very efficiently the design of the PCB becomes crucial. The number of vias needs to be optimized and the plating thickness should be >= 35 µm.

Fig. 9 and Fig. 10 show the results of a measurement and a simulation. The results show that with the used cooling systems and forced convection a thermal resistance of 10 K/W is feasible. This means for an ambient temperature of 40°C and a maximum junction temperature of 110°C a maximum power dissipation of 7W.

Comparing a SMD package to a THD package cooling the main difference comes from the heat conduction through the PCB. The heat conduction resistance through the PCB is in the range of 1 – 3 K/W. Since the

THD is directly connected to the TIM this resistance is not existingt. One has also to consider that THD usually have a quite big and thick leadframe which improves the heat spreading and finally increase the effective heat conduction area through the TIM (reduced Rth_TIM).

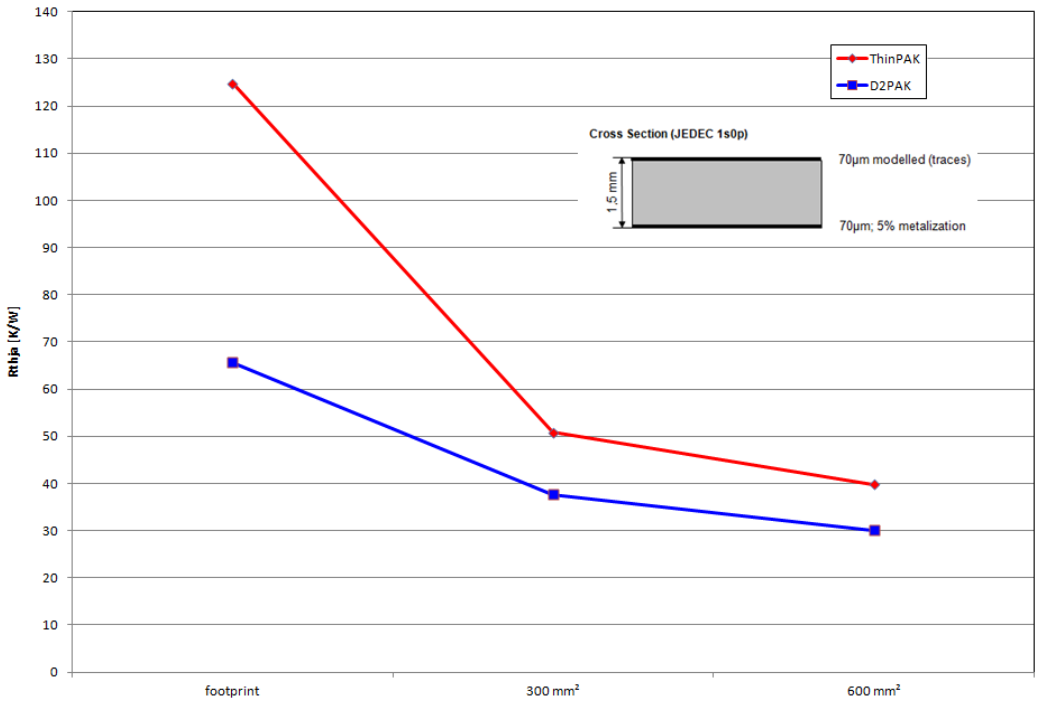

Fig. 6: Thermal simulation: Thermal resistance Rthja depending on copper area

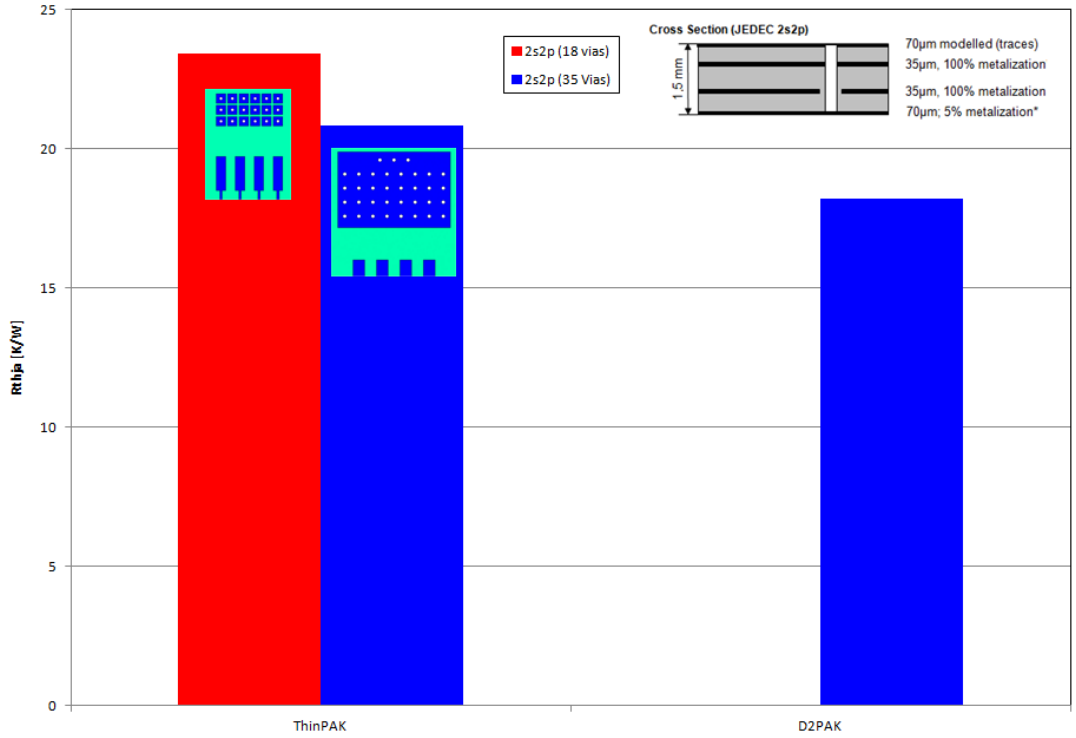

Fig. 7: Thermal simulation: Thermal resistance Rthja (PCB size: 76.2 × 114.3 × 1.5 mm³, via = 0.3 mm; plating 25 µm; 18 pcs. / 35 pcs.)

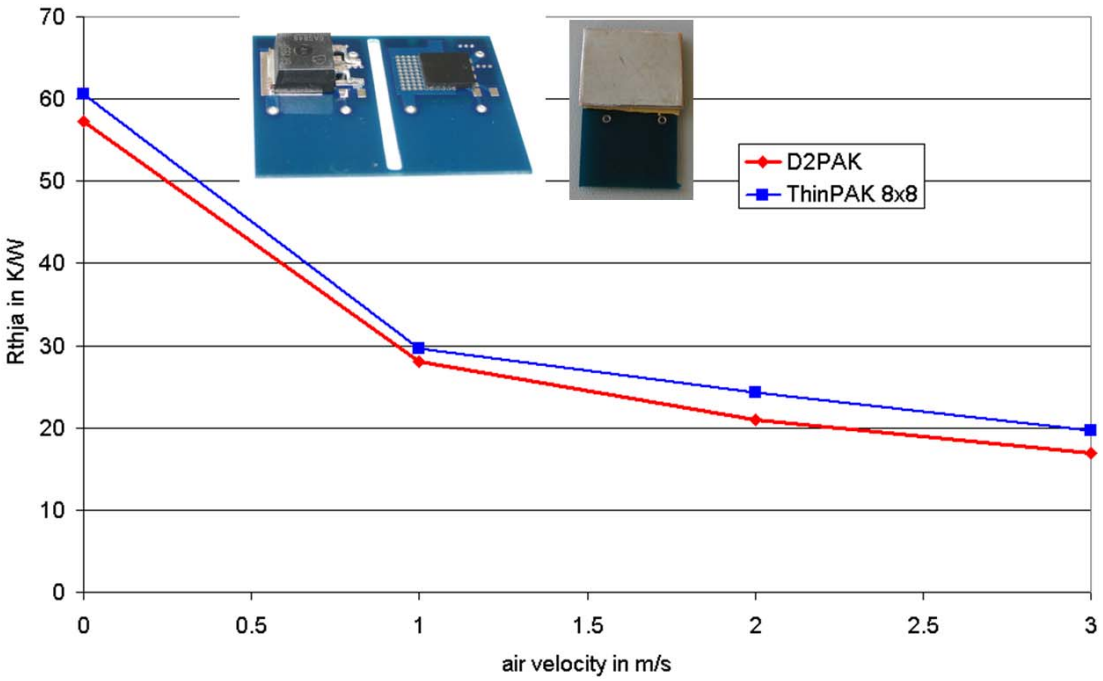

Fig. 8: Thermal measurement Rthja for ThinPAK and D^{2}PAK (Plate heatsink)

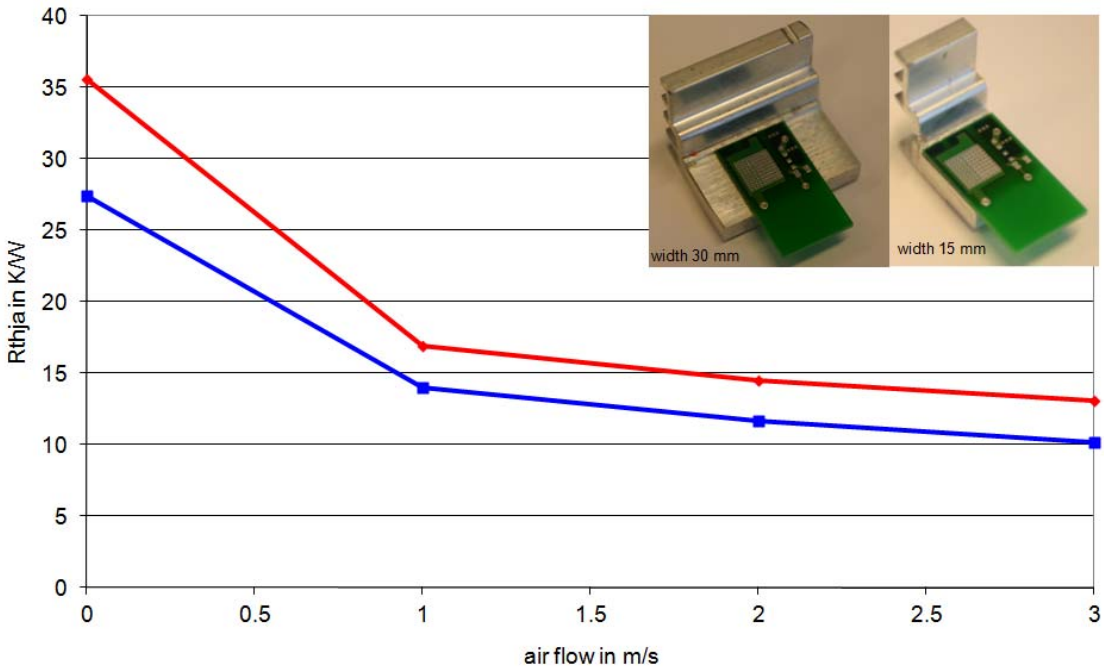

Fig. 9: Thermal measurement Rthja for ThinPAK (heatspreader and extrusion heatsink)

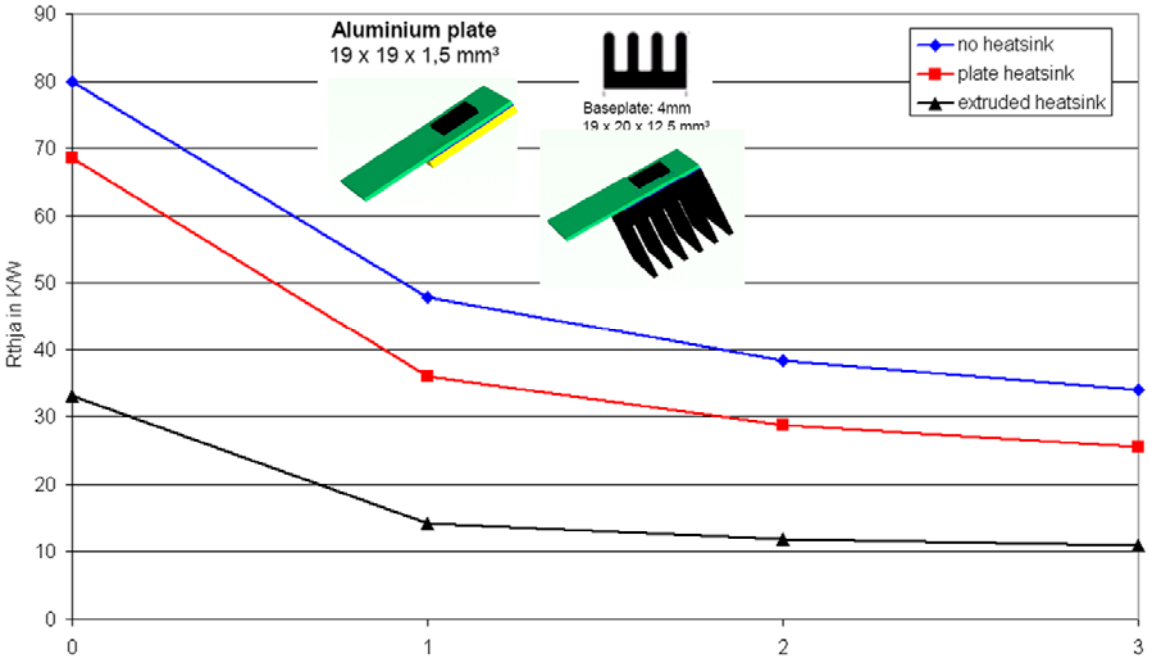

Fig. 10: Thermal simulation for ThinPAK: without heatsink, plate heatsink and extrusion heatsink

5 Summary

The ThinPAK 8x8 is a leadless package which features tremendously reduced packages size and source inductivity. For an optimized cooling adaption of standard SMD cooling using a heatsink at the bottom side of the PCB is needed. Using such a cooling system up to 7W can be dissipated using reasonable heatsink sizes and forced convection. Comparing the ThinPAK to the D^2PAK using a proper PCB design the thermal performance is ~ 10% worse.