Solution Brief

FPGA

Intel® Agilex™ 5 FPGAs E-Series Deliver Cost-Effective Power and Performance for the Embedded Edge

Intel 7 process technology, high-level system integration and 2nd generation Intel® Hyperflex™ FPGA Architecture deliver the edge-centric Intel Agilex 5 FPGA E-Series

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Executive Summary

Edge applications require devices that deliver increasing amounts of data processing while consuming less power and occupying smaller footprints. Edge-deployed cloud usage models involve massive increases in data acquisition, local processing, and analytics. Industry 4.0 and IoT-driven "Connected -Everything" have ushered in the promise of autonomous operation, paving the way for new applications. However, this has simultaneously fueled demand for even greater performance in existing applications and put a greater emphasis on functional safety. The new Intel® Agilex™ 5 FPGAs E-Series leverage fabric, processors, I/O and specialized signal processing blocks to make it easy for customers to address these workloads effectively.

The product will deliver dramatic performance, capability, and efficiency increases, as well as provide integration and supply longevity with 15+ year product availability to meet market demands is common. These applications range from multi-axis drive systems to programmable logic controllers, robotics controllers and Autonomous Mobile Robots (AMRs). The E-Series FPGAs deliver heterogeneous computing capabilities and an extensive set of connectivity features to serve diverse markets such as industrial networking, broadcast, medical and test and measurement.

Intel Agilex 5 FPGA E-Series Elements

Power-Efficient Performance

The E-Series FPGA is designed to target lower power and higher performance than previous generations of Intel edge-centric FPGAs. Its performance is 2.5 times (50 % total lower power) compared to the Cyclone® V FPGAs. The power capabilities are accomplished through the use of the 2nd generation Intel Hyperflex FPGA Architecture combined with Intel 7 process technology where transistors are optimized for performance per watt.

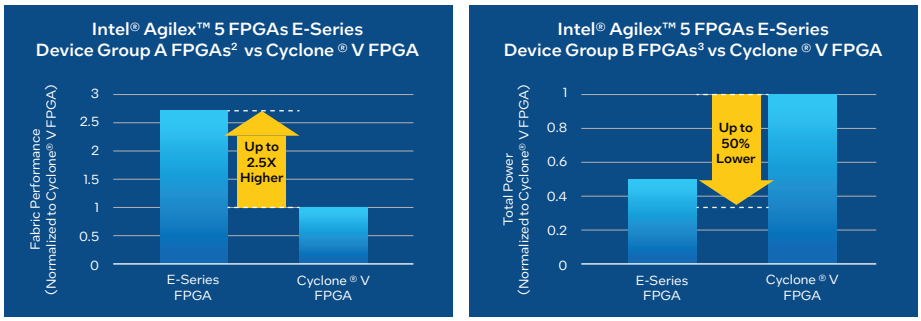


Figure 1. Intel® Agilex™ 5 FPGAs E-Series is up to 2.5X higher fabric performance or up to 50% lower total power compared to Cyclone® V FPGA[1]

Enhanced DSP with AI Tensor Block

The DSP blocks incorporated into the programmable-logic fabric of Intel Agilex 5 devices inherit the design of the variable-precision DSP blocks in the Intel® Agilex™ 7 device family. In addition to those capabilities, the DSP blocks in Intel Agilex 5 devices add features derived from the tensor block used in Intel® Stratix® 10 NX FPGAs. It is important to note that these new DSP blocks have been completely redesigned from the ground up to provide a 5X performance boost (see Table 1) while maintaining the same die size area compared to the prior generation of DSP blocks, thereby significantly increasing the performance-per-watt metric.

Applications	Multiplier	Capabilities per DSP Block		Improvement*
		Earlier Intel Agilex Devices	Enhanced DSP with AI Tensor Block*	
AI, Signal Processing	INT8	4 OPS	20 OPS	5X
	INT9	4 Multipliers	6 Multipliers	50%
Signal Processing	16-bit Complex Multiplier	Needs 2 DSP Blocks	1 DSP Block	2X

Table 1. The Enhanced DSP with AI Tensor block provides an order of magnitude increase in AI and DSP compute density.

*Available in Intel® Agilex™ 5 FPGAs D-Series and Intel® Agilex™ 5 FPGAs E-Series.

Hard Processor Subsystem

The hard processor system (HPS) is upgraded to an asymmetric multi-core Arm Cortex processor with 2xA55 and 2xA76. This approach allows for a mix-and-match of core types using Arm's DynamIQ technology. These processors operate with the DynamIQ Shared Unit (DSU) to create a four-core cluster that allows the processors to run asynchronously to each other, giving a wider range of performance options. The microprocessor unit (MPU) complex leverages a Network-on-Chip (NoC) to allow sharing of peripheral components and external DRAM interfaces. The Secure Device Manager interfaces to the HPS system using existing interfaces such as the Intel Agilex SoC FPGA products.

Extensive Connectivity Features Set

E-Series FPGAs and SoCs are equipped with transceivers optimized for a wide variety of applications with data rates ranging from 1 Gbps up to 28.1 Gbps in non-return-to-zero (NRZ) mode. MIPI D-PHY is enabled with a D-PHY PCS layer soft IP and HSIO and supports two operational modes:

- Differential high-speed (HS)
- Single-ended low-power (LP)

Additionally, its HPS includes time-sensitive networking (TSN) endpoints supporting data rates from 10 Mbps to 2.5 Gbps. The device targets compatibility with the Industrial Automation TSN profile but can address the real-time networking needs of other markets including automotive, utility, and professional audio/video.

Functional Safety

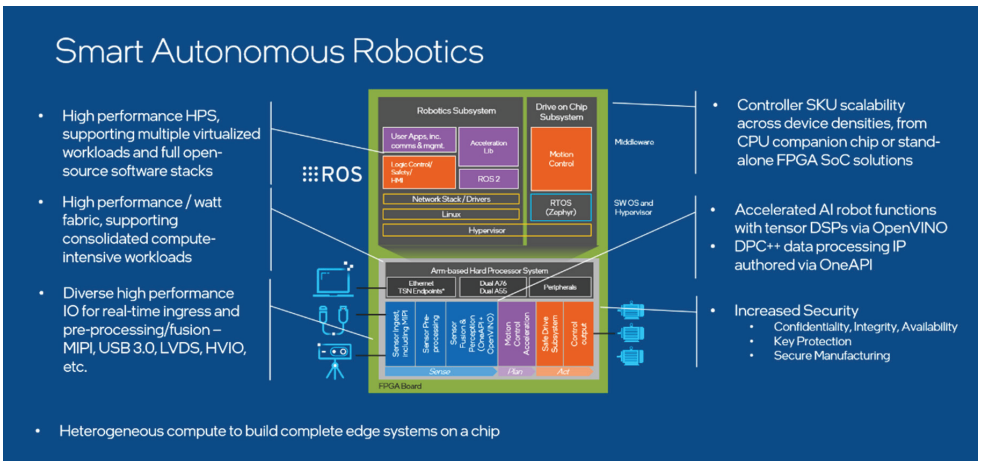
Intel Agilex 5 FPGAs and SoC FPGAs are produced using rigorous quality-controlled procedures and processes. The safety certification of Intel's tools, methodologies, and IPs is provided by a trusted, independent external review body, TÜV Rheinland, which is one of the world's leading testing service providers. TÜV independently verifies that Intel's systems, tools, and described methodologies are suitable for use in safety applications up to SIL3.

E-Series FPGA Workloads

Robotics

The Embedded Edge is also witnessing the arrival of smarter AI-driven robots, capable of collaboration and dynamic adjustment to any environment and task. The use of vision-guided robotics has given rise to the need for high-resolution and high-frame rate cameras. Custom Image Signal Processing (filtering, image rotation, 3D visions, photonics imaging, deep learning, etc.) is supported. The device enables emerging TSN industrial connectivity standards, with the implementation of a hardened TSN controller. At a high level, the containerization of applications and tasks produces a more efficient method of retrieving data from sensors and control loops into the processor; no time is lost in extra data processing.

For robotics applications, E-Series FPGA enables fast, deterministic closed-loop multi-axis motor control. This builds custom, low latency, and high-performance safety functionality. This feature addresses the trend to tighten control loops for faster, more precise control with the compute power for more axes in parallel.



Robotics

- Smarter AI-driven robots, capable of collaboration and dynamic adaption to environment and task
- 3D sensing technologies (Structured Light, Time-Of-Flight and Stereo)
- Rapid increase in use of Autonomous Mobile Robots in industrial process automation, warehouse, and beyond
- Multi-access connectivity to control and cloud, with coordination of heterogeneous AMR fleets

Figure 2. Robot-on-Chip: Sensor Ingest and Fusion for Autonomous Mobile Robots (AMRs) Diagram

Video and Vision

Next generation vision sensors use a wide variety of I/O standards that are constantly evolving, making interoperability and flexibility critical design requirements for video and vision systems. In addition to the interoperability and flexibility requirements, high-performance imaging systems have stringent size and power constraints as well. The E-Series FPGA addresses these complex design challenges with the following cutting-edge features:

- With new 2nd generation Intel Hyperflex FPGA Architecture that delivers on performance while optimizing for low power, the new performance-optimized E-Series FPGA delivers up to 1.37X higher fabric performance and up to 39% lower power as compared to Intel® Arria® 10 FPGA
  - Can comfortably run complex video designs at 300 MHz for 4K 60 fps video applications
- Integrated MIPI D-PHY support enabling MIPI CSI-2 and MIPI DSI-2 in low-power, high-speed (up to 2.5 Gbps) applications
- Support for the latest DisplayPort, HDMI, SLVS-EC, USB 3.1. DDR5 and PCIe 4, and up to 12G SDI connectivity standards
- Wide density range (up to 656 KLEs)
- Higher memory density than previous Cyclone® V devices
- Heterogeneous processing capabilities with Arm Cortex-A55 and Arm Cortex-A76 processors within the Hard Processor System (HPS)

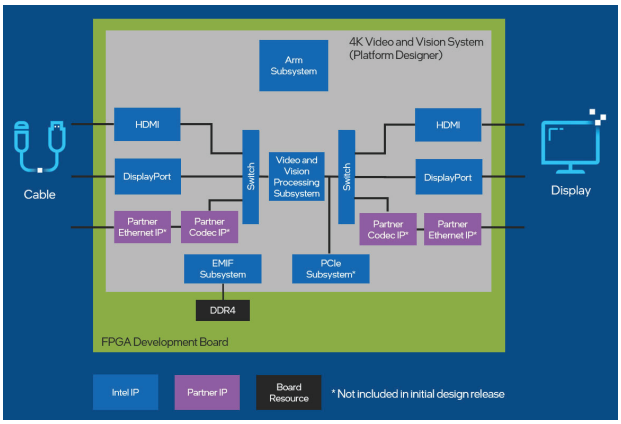


Figure 3. 4K Video and Vision Diagram

In addition to these hardware features, the E-Series FPGA is compatible with the Video and Vision Processing Suite of Intel® FPGA IP that leverages standard AXI-4 interfaces for easy plug-and-play with several advanced video processing IP blocks. Intel also offers an Image Sensor Processing (ISP) IP Subsystem that includes debayering, pixel defect correction, vignette correction, adaptive noise reduction, and white balance capabilities, to name a few. ISP makes use of an Arm-hosted graphical user interface that controls video processing functions and high-performance embedded direct memory access (DMA) in an intuitive, user-friendly way.

Motor Drives

Motor drives also need faster compute for simultaneous, multiple axes. The need to switch between different high-speed transistors, which requires deterministic connectivity to the outside world (i.e. TSN workload) and interoperability (OPC-UA) with other machinery.

E-Series FPGAs can generate greater CPU performance and fabric performance for multi-axes loads and multiple workloads. These workloads include drive control, HMI, and deterministic connectivity (TSN), OPC-UA, CPU, and I/Os. Its ability to drive new technology power transistors allows faster switching I/O. The device executes increasingly complex safety monitoring functions via the powerful HPS and integrated functional safety diagnostics. The E-Series FPGA executes sophisticated control and AI, supported by the tensor digital signal processor (DSP).

Drive-On-Chip Case Study

E-Series FPGAs can directly process multiple incoming signals and implement hardware-level deterministic and parallel control. This enables power switches to function faster and conserve more power through reduced switching time and lower resistance when switched on. Since they switch faster, the switching signals to control them must be delivered with improved time resolution and switching dynamics to respond quickly to transient source and load behavior. This approach allows a so-called “Drive-on-chip” solution that can address many market needs, for example, Industrial multi-axis control, battery charging, or robotics.

Features include:

- CPU subsystem configured for multi-axis motor control applications
- Arithmetic IP modules implemented in FPGA resources for algorithm acceleration
- Dedicated FPGA drives control logic that allows interfacing with power electronics
- Performance counters for precise analysis and control of time-sensitive control functions
- Flexible architecture to allow different external interfaces for communications, encoder types, motor types
- Ability to scale the design for single to multiple motor axes
- High performance, low power implementation on E-Series FPGAs
- Modular subsystem design approach

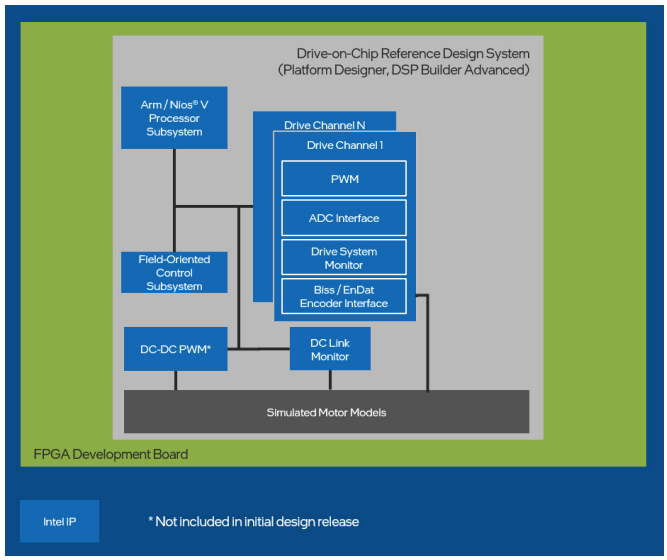


Figure 4. Drive-on-Chip Diagram

Programmable Logic Controllers

Programmable Logic Controllers (PLCs) need faster compute at the Edge. This is driven by shorter cycle-time requirements and the consolidation of multiple workloads in one device such as: compute, control, HMI, cloud-connectivity, and safety. E-Series FPGAs can run concurrent critical workload consolidation enabled by quad-core (hard processor system) HPS and multi-processing.

Additionally, its fabric performance and I/Os easily compute/control HMI and deterministic connectivity (TSN) and interoperability (OPC-UA). The device can handle sophisticated AI and MPC control algorithms and execute increasingly complex safety monitoring functions via powerful hard processor system HPS and integrated functional safety diagnostics. E-Series FPGA executes sophisticated control and AI, supported by tensor DSP.

Sample Use Cases

E-Series FPGA suits a wide range of applications from the embedded edge to deployed cloud usage models where there is a massive increase in data acquisition, local processing, and analytics.

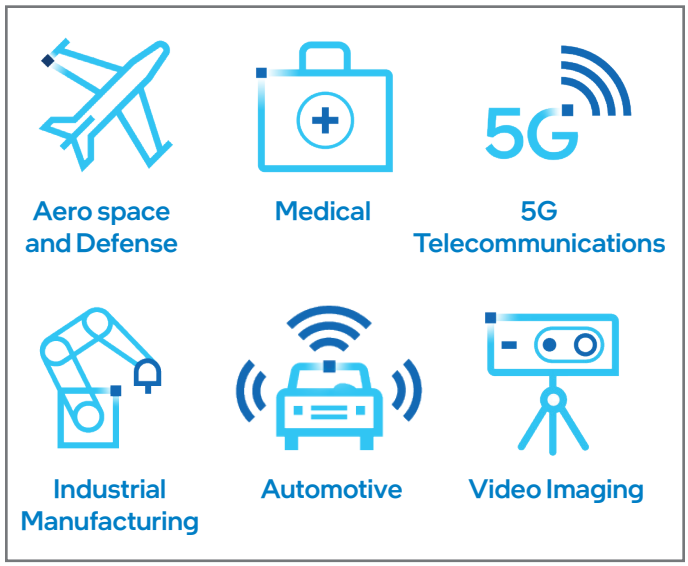


Figure 5. Example applications for Intel Agilex 5 FPGAs E-series

Conclusion

Many embedded applications require deterministic connectivity, low latency, and interoperability together with a high-performance-compute architecture to handle the ever-increasing amounts of data that need to be processed. E-Series FPGAs contain a wide variety of features, such as power-efficient, high-performance FPGA fabric, enhanced DSP with AI Tensor Block, HPS, and extensive set of connectivity options that support these next generation embedded applications while requiring lower power consumption and less board space. It implements reliable and secure systems with functional safety to offer advanced security features in a single device family.

[1] Fabric performance comparison is done on mid speed grades for E-Series FPGA and Cyclone® V FPGA, while total power comparison is done on the equivalent speed performance for E-Series FPGA and Cyclone® V FPGA

[2] Device Group A FPGAs is at 0.8 V when compared with Cyclone V FPGA.

[3] Device Group B FPGAs is at 0.75 V, 100% fabric utilization, and 350 MHz when compared with Cyclone V FPGA.

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