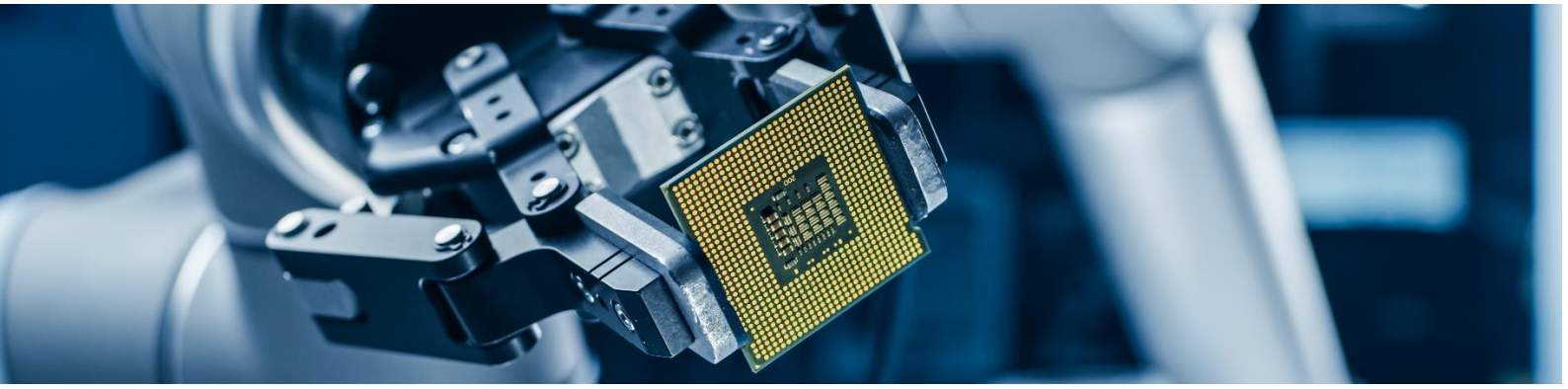
Event Invitation



Building a RISC-V system running El Caminos Machine Code Monitor on a Lattice FPGA

21st April 2021 – online

In times of fast evolution, staying at the cutting edge of technology is only achievable by continuous learning. With this seminar, Arrow provides you the chance for a job specific training.

The typical design flow when using Lattice FPGAs is to combine IP blocks with custom logic written in VHDL or Verilog. Some functionality however is better implemented in software because this is more flexible and the performance of a pure hardware implementation might not be required.

With the new RISC-V MC CPU IP core it is now easy to add a softcore CPU to the design and achieve the optimum mix between hardware performance and software flexibility.

In this seminar we will learn how to implement a basic RISC-V system in a MachXO3D FPGA and add some software that is executed at power-up. The El Camino machine code monitor used in this example, enables the communication with the system through a serial connection and a standard terminal program running on a host computer. The monitor allows to read or write memory as well as download data or code independent of a debugger installation. It can be used as a template for implementing your own, low-level menu or command driven interface to your FPGA based processor system.

Speakers: Wolfgang Loewer (CTO, El Camino GmbH)
Language: English
Prerequisites: none
Seminar Actions: Presentation, Software Demo
Contact Person: Harald Fluegel, hfluegel@arroweurope.com, +49 151 – 14 05 10 42

Agenda (Time zone: CEST)

10:00 – 10:05	Welcome
10:05 – 10:20	Introduction to softcore CPUs and RISC-V
10:20 – 10:50	Demo of building and running a RISC-V system with El Caminos Machine Code Monitor
10:50 – 11:00	Questions & Answers

Register